

 ICOM

SERVICE MANUAL

UHF TRANCEIVER

IC-F40GT
IC-F40GS
IC-F41GT
IC-F41GS

INTRODUCTION

This service manual describes the latest service information for the IC-F40GT/GS and IC-F41GT/GS UHF TRANSCEIVERS at the time of publication.

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 10 V. This will ruin the transceiver.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1110001810	S.IC TA7368F	IC-F40GT	MAIN UNIT	1 piece
8930053170	2337 Key board	IC-F41GS	CHASSIS	5 pieces

Addresses are provided on the inside back cover for your convenience.



REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 40 dB or 50 dB attenuator between the transceiver and a deviation meter or spectrum analyser when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

EXPLICIT DEFINITIONS

FREQUENCY COVERAGE

L-band	400–430 MHz
ML-band	440–480 MHz
MH-band	450–490 MHz
H-band	480–512 MHz
	480–520 MHz

CHANNEL SPACING

Wide/Narrow-type	25 kHz/12.5 kHz
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SECTION 1 SPECIFICATIONS

	USA	GEN/EUR
GENERAL	Measurement method	EIA-152-C/204D
	Frequency coverage	400.000–430.000 MHz [L-band] 440.000–480.000 MHz [ML-band] 450.000–490.000 MHz [MH-band] 480.000–512.000 MHz [H-band]
	Type of emission	16K0F3E [25 kHz; Wide], 8K50F3E [12.5 kHz; Narrow]
	Number of conventional channels	Max. 256 ch (16 channels × 16 banks)
	Power supply requirement	7.2 V DC (negative ground; supplied battery pack)
	Current drain (approx.)	TX at High 2.0 A Rx rated audio 300 mA stand-by 95 mA (typical)
	Frequency error	2.5 ppm
	Usable temperature range	−30°C to +60°C (−22°F to +140°F)
	Dimensions (proj. not included)	54(W) × 139(H) × 38(D) mm; 21½(W) × 5½(H) × 1½(D) inch
	Weight (with BP-210)	420 g; 14.8 oz
TRANSMITTER	RF output power	4 W / 2 W / 1 W (High/Low2/Low1)
	Modulation system	Variable reactance frequency modulation
	Maximum permissible deviation	±5.0 kHz [Wide], ±2.5 kHz [Narrow]
	Spurious emissions	73 dBc typical
	Adjacent channel power	70 dB [Wide], 60 dB [Narrow]
	Audio frequency response	+2 dB to −8 dB of 6 dB/octave range from 300 Hz to 3000 Hz [Wide]/2550 Hz [Narrow]
	Audio harmonic distortion	3% typical at 1 kHz, 40% deviation
	FM hum and noise (typical)	46 dB [Wide], 40 dB [Narrow]
	Residual modulation	—
	Limitting charact of modulator	60–100% of max. deviation
RECEIVER	Ext. microphone connector	9-pin multi connector/2.2 kΩ
	Receive system	Double-conversion superheterodyne system
	Intermediate frequencies	1st: 47.25 MHz, 2nd: 450 kHz
	Sensitivity (typical)	0.25 µV at 12 dB SINAD
	Squelch sensitivity (at threshold) (typical)	0.25 µV
	Adjcent channel selectivity (typical)	73 dB [Wide], 63 dB [Narrow]
	Spurious response	70 dB
	Intermodulation (typical)	74 dB
	FM hum and noise (typical)	46 dB [Wide], 40 dB [Narrow]
	Hum and noise (with CCITT filter) (typical)	—
Audio output power (at 7.2 V DC)		500 mW typical at 5% distortion with a 8 Ω load 600 mW typical at 5% distortion with a 6 Ω load
External SP connector		9-pin multi connector/8 Ω

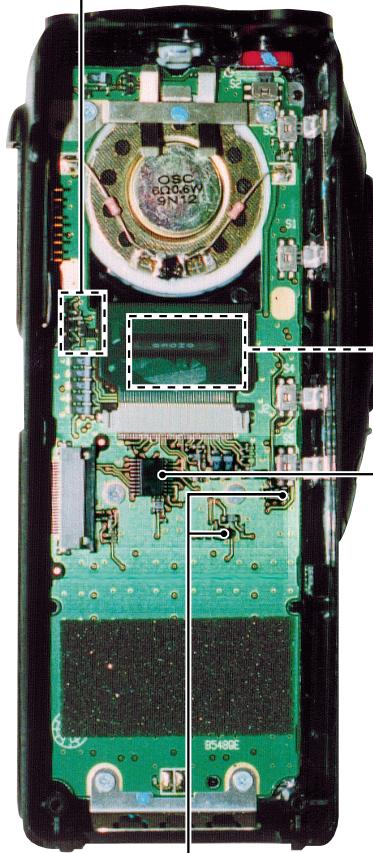
All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

• FRONT UNIT

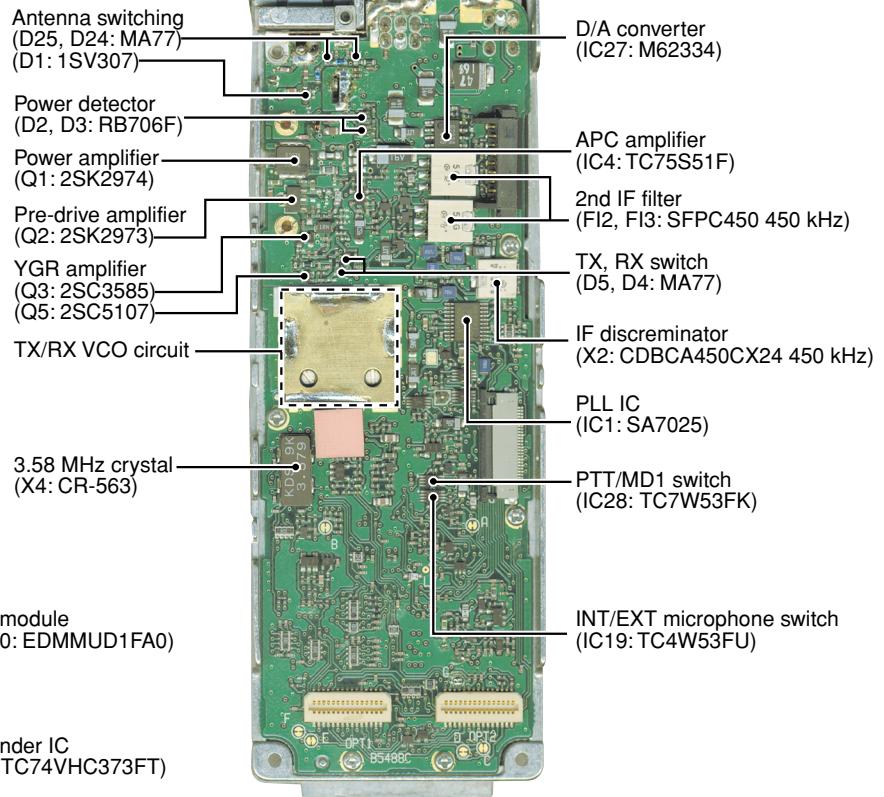
Bottom view

Internal speaker switch circuit
(Q6, Q7: CPH3403, Q8: 2SC4081,
Q9: DTC144EUA)



• MAIN UNIT

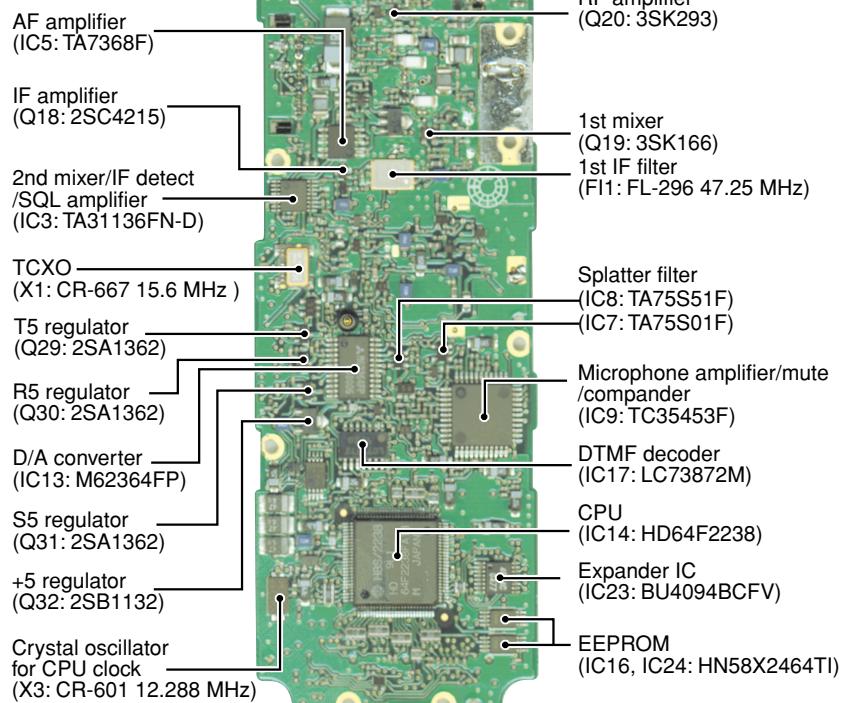
Top view



• MAIN UNIT

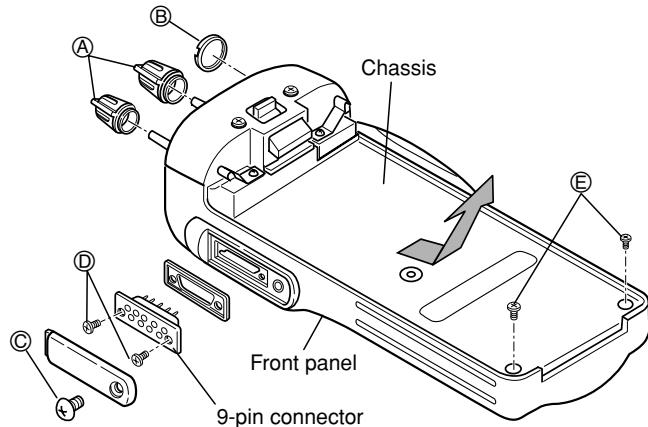
Bottom view

KEY LED switch
(Q1, Q2: 2SC4116BL)



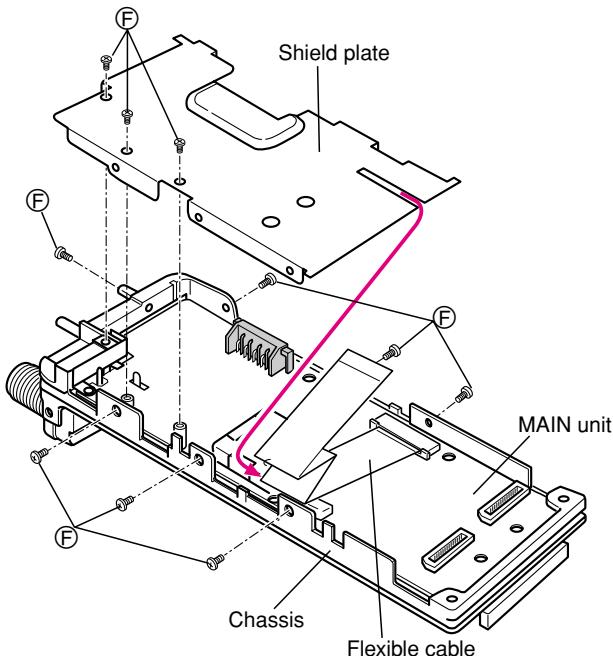
SECTION 3 DISASSEMBLY INSTRUCTIONS

1 Removing the chassis panel



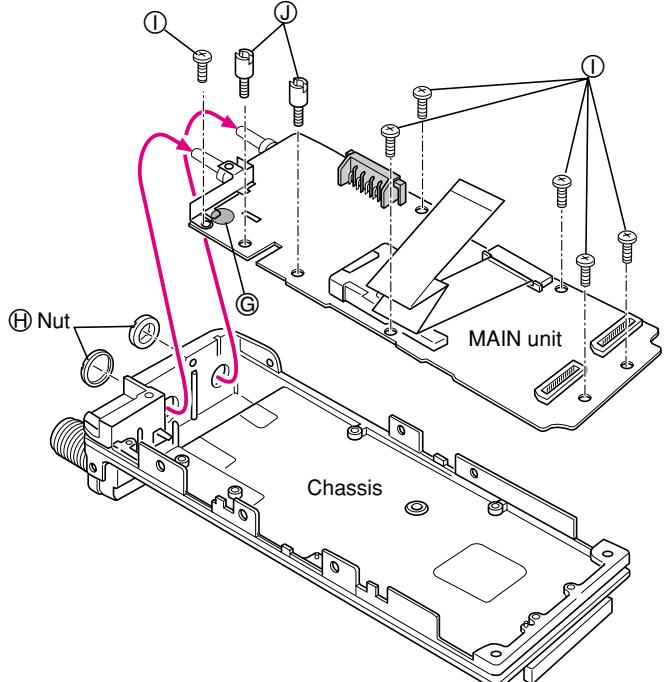
- ① Remove 2 knobs Ⓐ, and unscrew 1 nut Ⓑ.
- ② Unscrew 1 screw Ⓒ (ICOM screw), and 2 screws Ⓓ (2 × 4 mm, black) from the 9-pin connector.
- ③ Unscrew 2 screws Ⓔ (2 × 8 mm, silver) from the chassis.
- ④ Take off the chassis in the direction of the arrow.

2 Removing the shield plate



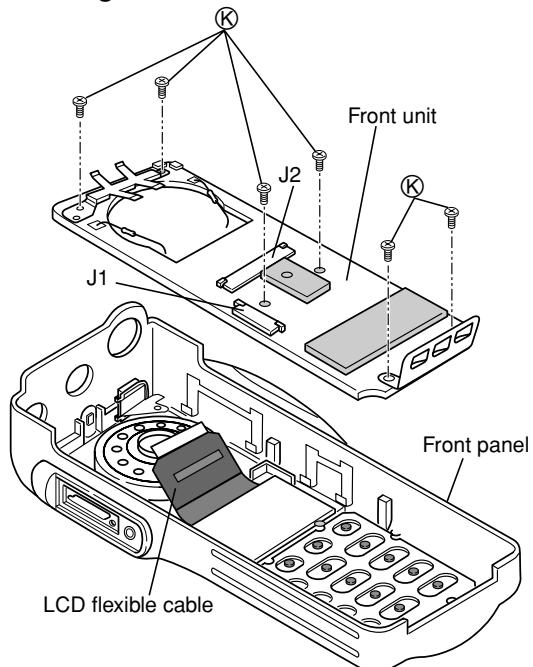
- ① Unplug the flexible cable from J1 on the FRONT unit to separate the chassis.
- ② Take off the flexible cable in the direction of the arrow.
- ③ Unscrew 10 screws Ⓕ (2 × 3 mm, black) to separate the shield plate.

3 Removing the MAIN unit



- ① Unsolder 1 point Ⓖ at the antenna lead.
- ② Unscrew 2 nuts ⓪.
- ③ Unscrew 6 screws ⓘ (2 × 4 mm, silver), and 2 screws ⓙ from the MAIN unit.
- ④ Take off the MAIN unit in the direction of the arrow.

4 Removing the FRONT unit



- ① Unplug the LCD flexible cable from J2 on the FRONT unit to separate the front panel.
- ② Unscrew 6 screws ⓫ (2 × 3.5 mm, silver) from the FRONT unit.
- ③ Unsolder the leads of speaker.

SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. The circuit does not allow transmit signals to enter receiver circuits.

Received signals enter the antenna connector (CHASSIS; J1) and pass through the low-pass filter (L1, L2, C1, C2, C420). The filtered signals are passed through the $\frac{1}{4}$ type antenna switching circuit (D25, D24, L39) and then applied to the RF circuit.

4-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the tunable bandpass filter (D21, L38). The filtered signals are amplified at the RF amplifier (Q20) and then passed through the another three-stage bandpass filters (D20–D18, L36, L34, L33) to suppress unwanted signals. The filtered signals are applied to the 1st mixer circuit.

D18–D21 employ varactor diodes, that are controlled by the CPU via the D/A converter (IC27), to track the bandpass filter. These varactor diodes tune the center frequency of an RF pass band for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal into fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only the desired frequency passes through a monolithic filter at the next stage of the 1st mixer.

The RF signals from the bandpass filter are mixed with the 1st LO signals, where come from the RX VCO circuit via the attenuator (R108–R106), at the 1st mixer circuit (Q19) to produce a 47.25 MHz 1st IF signal. The 1st IF signal is passed through a monolithic filter (FI1) in order to obtain selection capability and to pass only the desired signals. The filtered signal is applied to the 2nd IF circuit after being amplified at the 1st IF amplifier (Q18).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. The double-conversion superheterodyne system (which convert receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

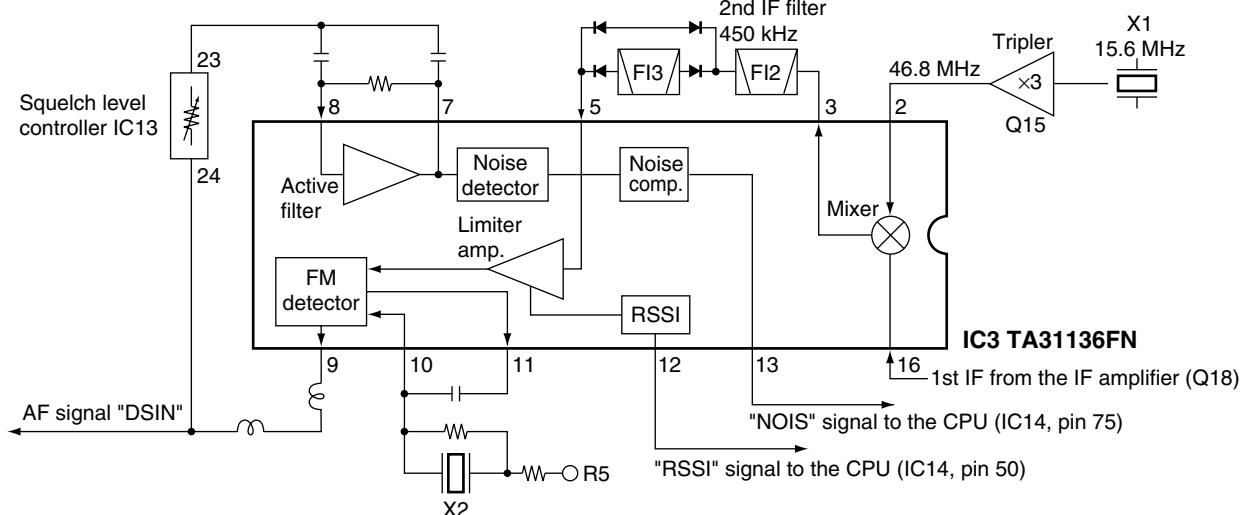
The 1st IF signal from the IF amplifier (Q18) is applied to the 2nd mixer section of the FM IF IC (IC3, pin 16), and is mixed with the 2nd LO signal to be converted into a 450 kHz 2nd IF signal.

The FM IF IC (IC3) contains the 2nd mixer, 2nd local oscillator, limiter amplifier, quadrature detector, active filter and noise amplifier circuits. A 2nd LO signal (46.8 MHz) is produced at the PLL circuit by tripling its reference frequency (15.6 MHz).

The 2nd IF signal from the 2nd mixer (IC3, pin 3) passes through the ceramic filters (FI2, FI3) during narrow channel spacing selection or FI2 only (bypassing FI3) during wide channel spacing selection to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier section (IC3, pin 5) and applied to the quadrature detector section (IC3, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

The demodulated AF signals are output from pin 9 (IC3) and applied to the AF circuit via the receiver mute circuit.

• 2nd IF and demodulator circuits



4-1-5 AF AMPLIFIER CIRCUIT

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

The AF signals from the FM IF IC (IC3, pin 9) are amplified at the AF amplifier section of the compander IC (IC9, pins 5, 4) and are then applied to the high-pass filter circuit (IC10).

The high-pass filter characteristics are controlled by the FSW signal from the I/O expander IC (IC23, pin 14). When FSW signal is high, the cut-off frequency is shifted higher to remove CTCSS or DTCS signals.

The filtered AF signals from the high-pass filter (IC10, pin 4) are applied to the de-emphasis section of compander IC (IC9, pin 3) with frequency characteristics of -6 dB/octave, and are then passed through the low-pass filter, high-pass filter, expander sections of compander IC (IC9). The output signal from IC9 (pin 38) is applied to the electronic volume controller (IC13, pin 1).

The output AF signals from the electronic volume controller (IC13, pin 2) are applied to the AF power amplifier (IC5) to drive the speaker.

4-1-6 RECEIVE MUTE CIRCUITS

• NOISE SQUELCH

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some noise components in the AF signals from the FM IF IC (IC3, pin 9) are passed through the level controller (IC13, pins 24, 23). The level controlled signals are applied to the active filter section in the FM IF IC (IC3, pin 8). Noise components about 10 kHz are amplified and output from pin 7.

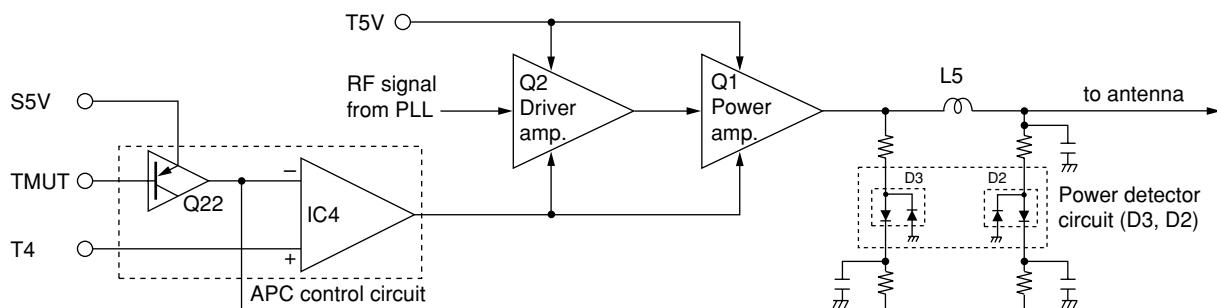
The filtered signals are converted into the pulse-type signals at the noise detector section and output from pin 12 (NOIS).

The NOIS signal from the FM IF IC is applied to the CPU (IC14, pin 75). The CPU then analyzes the noise condition and controls the AF mute signal via "AFMT" line (IC23, pin 13) to the AF regulator (Q23, Q24).

• CTCSS AND DTCS

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS or DTCS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

• APC circuit



A portion of the AF signals from the FM IF IC (IC3, pin 9) passes through the low-pass filter (IC20b/a) to remove AF (voice) signals and is applied to the CTCSS or DTCS decoder inside the CPU (IC14, pin 46) via the "RXDT" line to control the AF mute switch via the I/O expander IC (IC23).

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals within +6 dB/octave pre-emphasis characteristics from the microphone to a level needed for the modulation circuit.

The AF signals (MIC+) from the FRONT unit via J3 (pin 22) are passed through the internal/external microphone switch (IC19, pins 7, 1) and level controller (IC13, pins 9, 10) to the microphone amplifier circuit.

The AF signals from the level controller (IC13) are applied to the microphone amplifier section of compander IC (IC9, pin 12). The amplified signals are passed through the compressor, low-pass filter and high-pass filter sections of IC9.

The filtered AF signals are amplified at the buffer amplifier (Q47) and pre-emphasized with +6dB/octave at the pre-emphasis circuit (R166, C203), and are then applied to the IDC amplifier section of IC9 (pin 8).

The amplified AF signals are passed through the limiter amplifier and low-pass filter sections of IC9 after being passed through the AF mute switch inside of IC9.

The output signals from pin 6 are passed through the splatter filter (IC8) and level controller (IC13, pins 21, 22), and are then applied to the modulation circuit (D7).

4-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The AF signals from the level controller (IC13) change the reactance of varactor diode (D7) to modulate the oscillated signal at the TX VCO circuit (Q12, D8). The modulated VCO signal is amplified at the buffer amplifiers (Q8, Q6) and is then applied to the drive amplifier circuit via the T/R switch (D4).

The CTCSS/DTCS signals from the CPU (IC14, pin 44) are passed through the low-pass filter (IC21), level controller (IC13, pins 12, 11) and mixer (IC7), and are then applied to the VCO circuit via the splatter filter (IC8).

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS

The drive/power amplifier circuits amplify the VCO oscillating signal to an output power level.

The signal from the VCO circuit passes through the T/R switch (D4), and is amplified at the YGR (Q5, Q3), drive (Q2), power (Q1) amplifiers to obtain 4 W of RF power (at 7.2 V DC).

The amplified signal is passed through the APC detector, antenna switching circuit (D1) and low-pass filter, and is then applied to the antenna connector.

The bias current of the drive (Q2) and power (Q1) amplifiers is controlled by the APC circuit.

4-2-4 APC CIRCUIT

The APC circuit (IC4, Q22) protects the drive and power amplifiers from excessive current drive, and selects output power of HIGH, LOW2 or LOW1.

The APC detector circuit detects forward signals and reflection signals at D3 and D2 respectively. The combined voltage is at a minimum level when the antenna impedance is matched at $50\ \Omega$ and is increased when it is mismatched.

The detected voltage is applied to the differential amplifier (IC4, pin 3), and the "T4" signal from the D/A converter (IC27, pin 4), controlled by the CPU (IC14), is applied to the other input for reference. When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the differential amplifier (IC4, pin 4) controls the input current of the drive amplifier (Q2) and power amplifier (Q1) to reduce the output power.

4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the TX/RXVCO circuit (Q12, Q11). The oscillated signal is amplified at the buffer amplifiers (Q8, Q7) and then applied to the PLL IC (IC1, pin 5).

The PLL IC contains a prescaler, programmable counter, programmable divider and phase detector, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

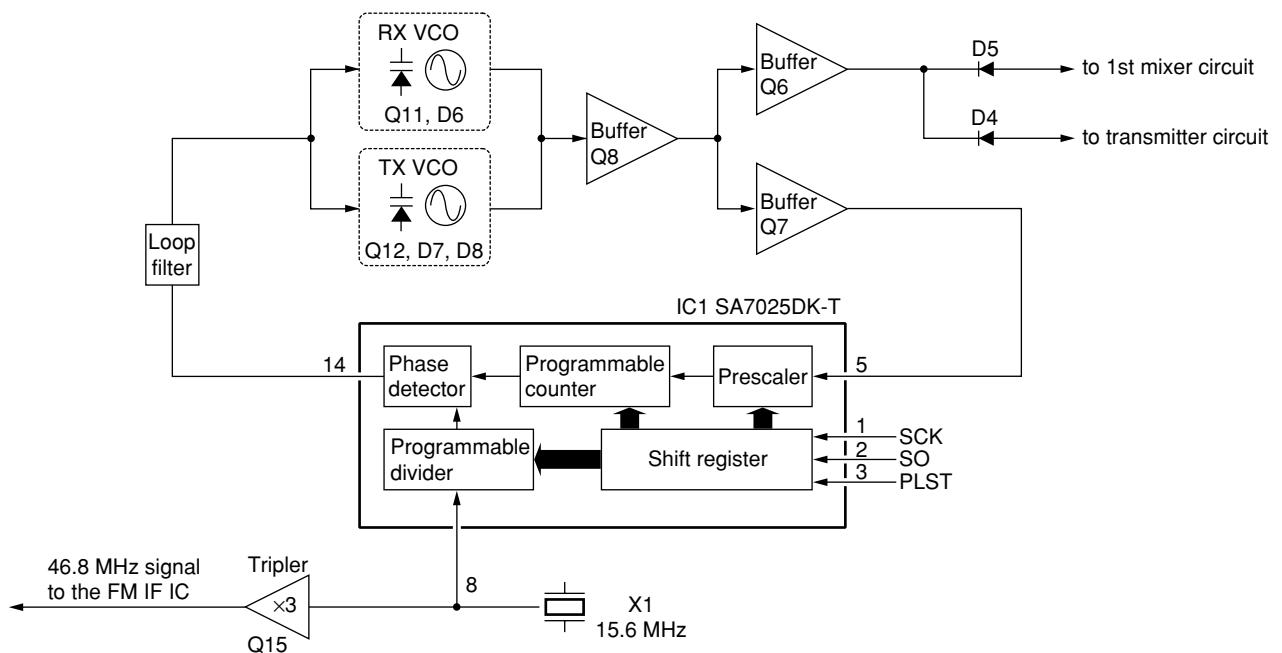
If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

4-3-2 VCO CIRCUIT

The VCO circuit contains a separate RX VCO (Q11, D6) and TX VCO (Q12, D7, D8). The oscillated signal is amplified at the buffer amplifiers (Q8, Q6) and is then applied to the T/R switch (D5, D4). Then the receive 1st LO (Rx) signal is applied to the 1st mixer (Q19) and the transmit (Tx) signal to the YGR amplifier circuit (Q5).

A portion of the signal from the buffer amplifier (Q8) is fed back to the PLL IC (IC1, pin 5) via the buffer amplifier (Q7) as the comparison signal.

• PLL circuit



4-4 POWER SUPPLY CIRCUIT VOLTAGE LINE

LINE	DESCRIPTION
HV	The voltage from the attached battery pack.
VCC	The same voltage as the HV line (battery voltage) which is controlled by the power switch ([VOL] control).
CPU5V	Common 5 V converted from the VCC line by the reference regulator circuit (IC12). The output voltage is applied to the CPU (IC14), 5 V regulator circuit (Q32, Q33) and reset circuit (IC15).
+5V	Common 5 V converted from the VCC line by the +5V regulator circuit (Q32, Q33).
S5V	Common 5 V converted from the +5V line by the S5V regulator circuit (Q31).
T5V	5 V for transmitter circuits regulated by the T5V regulator circuit (Q29).
R5	5 V for receiver circuits regulated by the R5 regulator circuit (Q30).

4-5 PORT ALLOCATIONS

4-5-1 CPU (IC14)

Pin number	Port name	Description
4	RESB	Outputs reset signal for the expander IC (IC23).
5	RMUT	Input port for AF mute signal from the optional units via J1 or J2.
6	MMUT	Input port for MIC mute signal from the optional units via J1 or J2.
7	PTOT	Input port for the [PTT] switch Low : While [PTT] switch is pushed.
13	EXST	Outputs strobe signals to the expander IC (IC23).
15	APST	Outputs strobe signals to the compander IC (IC9).
16	DIN	Outputs serial data signals to the compander IC (IC9).
17, 18, 19	RGS1, RGS2, MSKE	Output control signal for the compander IC (IC9).
21	FCLR	Outputs reset signal for the compander IC (IC9).
22–25	CB10–CB13	Input ports for rotary selector [SEL].
26	VCOS	Outputs TX VCO/RX VCO switching signal for the VCO switch (Q9, Q10). High : While transmitting
28	PLST	Outputs strobe signals to the PLL IC (IC1).
29	ULCK	Input port for the PLL unlock signal. Low : PLL is unlocked.
34	SCK	Outputs clock signal for the PLL IC (IC1), compander IC (IC9), expander IC (IC23), D/A converter (IC13), etc.

Pin number	Port name	Description
35	SO	Outputs data signals for the PLL IC (IC1), compander IC (IC9), expander IC (IC23), D/A converter (IC13), etc.
36	DAST	Outputs strobe signals to the D/A converter (IC13).
39	DTAC	Output clock signal to the DTMF decoder (IC17).
43	SENC	Outputs single tone signal.
44	CTDA	Outputs CTCSS/DTCS tone signal.
45	SDEC	Single tone signal input port for decoding.
46	RXDT	CTCSS/DTCS signals input port for decoding.
47	AFVI	Input port for the volume control [VOL]. High : [VOL] is maximum clockwise.
49	LVIN	Input port for the PLL lock voltage.
50	RSSI	Input port for the RSSI detection.
59	RES	Input port for the reset signal.
68	DTSD	Outputs serial data signals to the DTMF decoder IC (IC17).
70	TMUT	Outputs transmit mute signal. Low : During unlock or while muted
71	R5C	Outputs R5 regulator control signal. Low: While receiving
73	T5C	Outputs T5 regulator control signal. Low: While transmitting
75	NOIS	Input port for noise signals (pulse-type) for noise squelch operation.
81	SDA	I/O port for data signals from/to the D/A converter (IC27).
82	MSO	I/O port for data signals from/to EEPROMs (IC16, IC24).
87	BEEP	Outputs beep audio signals.
94	MSCK	Outputs clock signal to EEPROMs (IC16, IC24).
95	SCL	Outputs clock signal to the D/A converter (IC27).

4-5-2 I/O EXPANDER (IC23)

Pin number	Port name	Description
4	BUSY	Outputs BUSY detection. Low : The channel is busy.
6	DUSE	Outputs low-pass filter cut-off frequency control signal when DTCS is activated.
7	W/N	Outputs IF bandwidth control signal. High : While IF bandwidth is narrow.
11	S5C	Outputs S5 regulator control signal.
12	SPCN	Outputs internal speaker select signal.
13	AFMT	Outputs control signal for the AF amplifier regulator circuit. High: While AF amp. is activated.
14	FSW	Outputs high-pass filter's characteristics select signal.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

When you adjust the contents on pages 5-5 to 5-7, SOFTWARE ADJUSTMENT, the optional CS-F30G ADJ ADJUSTMENT SOFTWARE (Rev. 1.0 or later), *OPC-966 JIG CABLE (modified OPC-966 CLONING CABLE) are required.

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.5 V DC Current capacity : 5 A or more	Audio generator	Frequency range : 300–3000 Hz Output level : 1–500 mV
FM deviation meter	Frequency range : DC–600 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 40 or 50 dB Capacity : 10 W or more
Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 300–600 MHz Output level : 0.1 µV–32 mV (−127 to −17 dBm)
Digital multimeter	Input impedance : 10 MΩ/V DC or better	DC voltmeter	Input impedance : 50 kΩ/V DC or better
RF power meter (terminated type)	Measuring range : 1–10 W Frequency range : 300–600 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
		AC millivoltmeter	Measuring range : 10 mV–10 V

■ SYSTEM REQUIREMENTS

- IBM PC compatible computer with an RS -232C serial port (38400 bps or faster).
- Microsoft Windows 95 or Windows 98
- Intel i486DX processor or faster (Pentium 100 MHz or faster recommended)
- At least 16 MB RAM and 10 MB of hard disk space
- 640×480 pixel display (800×600 pixel display recommended)

■ ADJUSTMENT SOFTWARE INSTALLATION

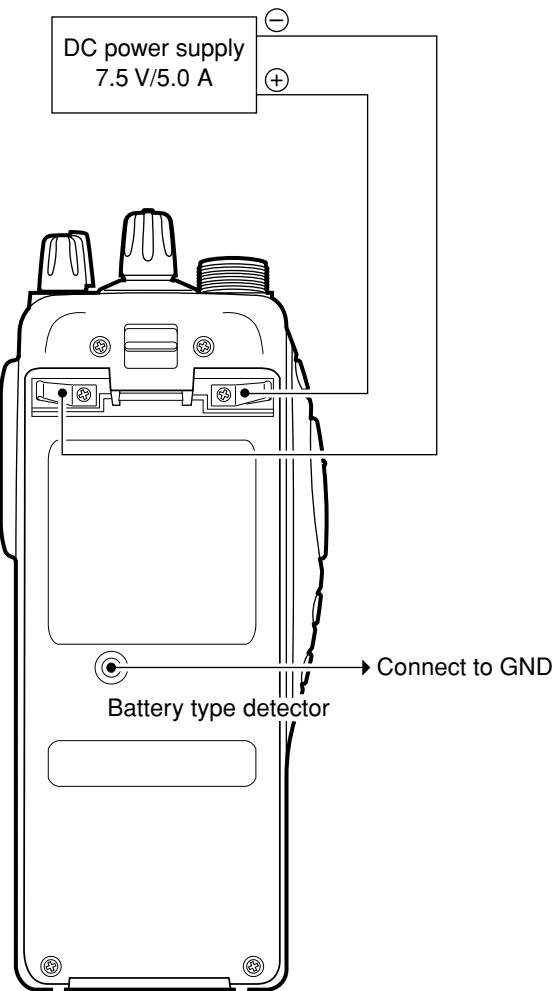
- ① Boot up Windows.
- Quit all applications when Windows is running.
- ② Insert the 'CS-F30G' into the appropriate drive.
- ③ Select 'Run' from the [Start] menu.
- ④ Type the setup program name using the full path name, then push [Enter] key.
(ex. D:\CSF30GADJ\disk1\Setup.exe)
- ⑤ Follow the prompts.
- ⑥ Program group 'CS-F30G ADJ' appears in the 'Programs' folder of the [Start] menu.

■ STARTING SOFTWARE ADJUSTMENT

- ① Connect IC-F40GT, F40GS, F41GT or F41GS and PC with *OPC-966 JIG CABLE.
- ② Turn the transceiver power ON.
- ③ Boot up Windows, and click the program group 'CS-F30G ADJ' in the 'Programs' folder of the [Start] menu, then CS-F30G ADJ's window appears.
- ④ Click 'Connect' on the CS-F30G's window, then appears IC-F40GT, F40GS, F41GT or F41GS's up-to-date condition.
- ⑤ Set or modify adjustment data as desired.

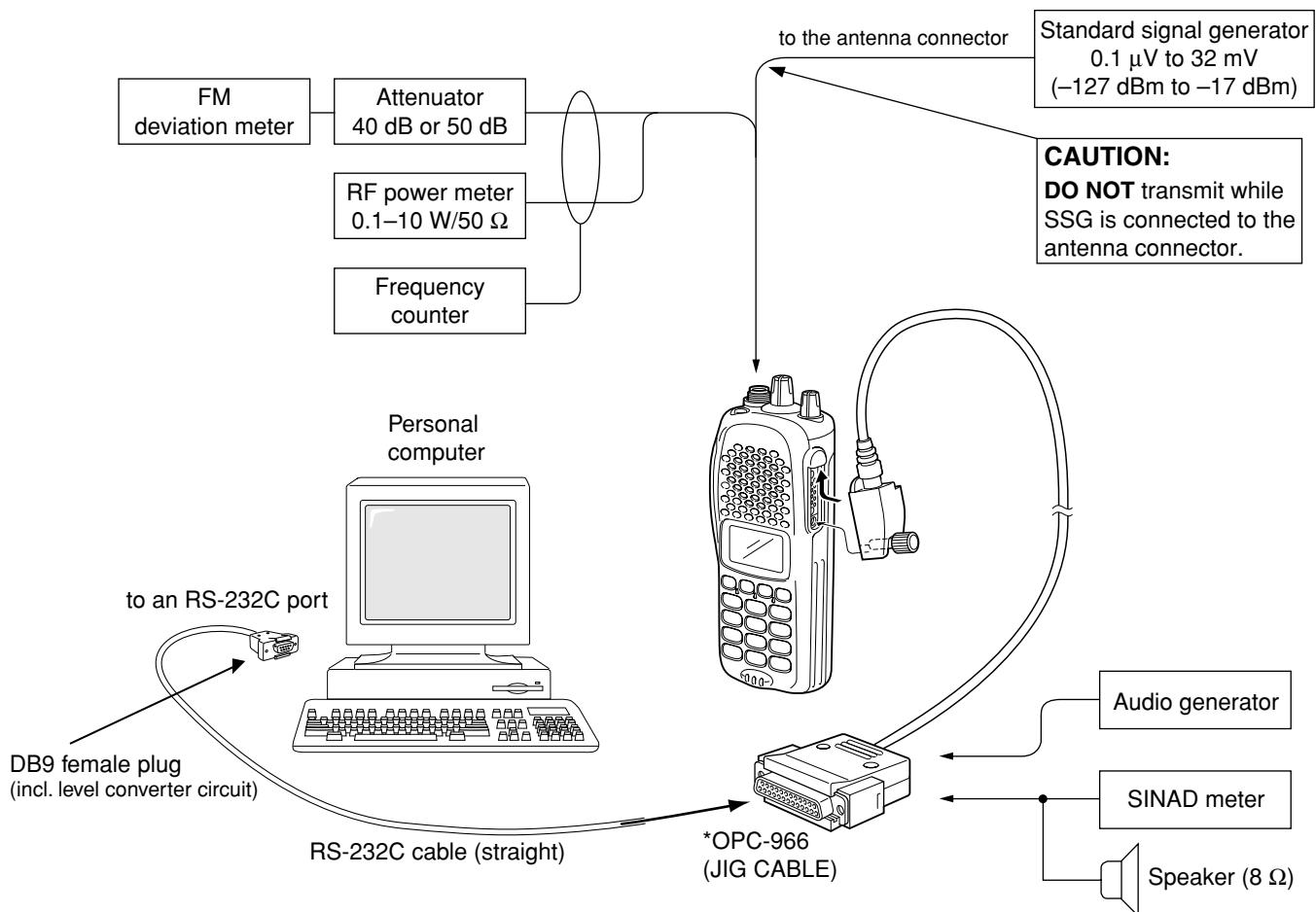
• High power transmission

When you adjust the output power (high power), the battery type detector must be connected to GND (see illustration at below). Otherwise the transceiver does not transmit high power, the output power will be low.

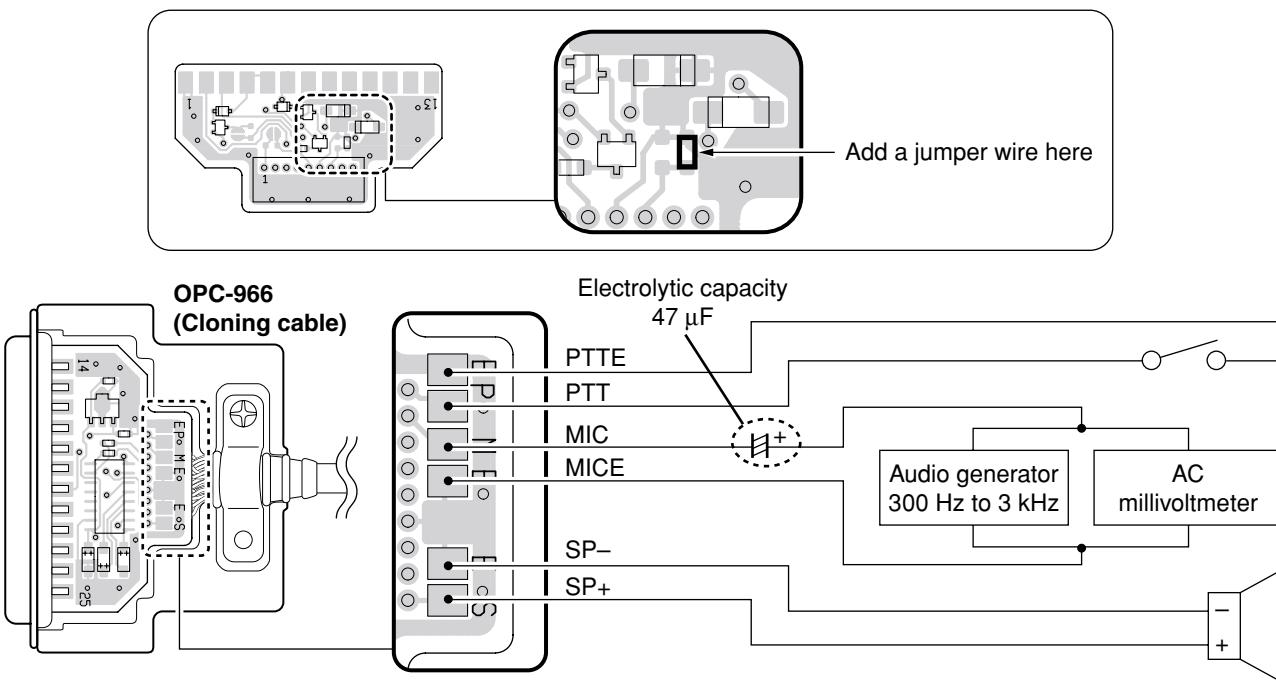


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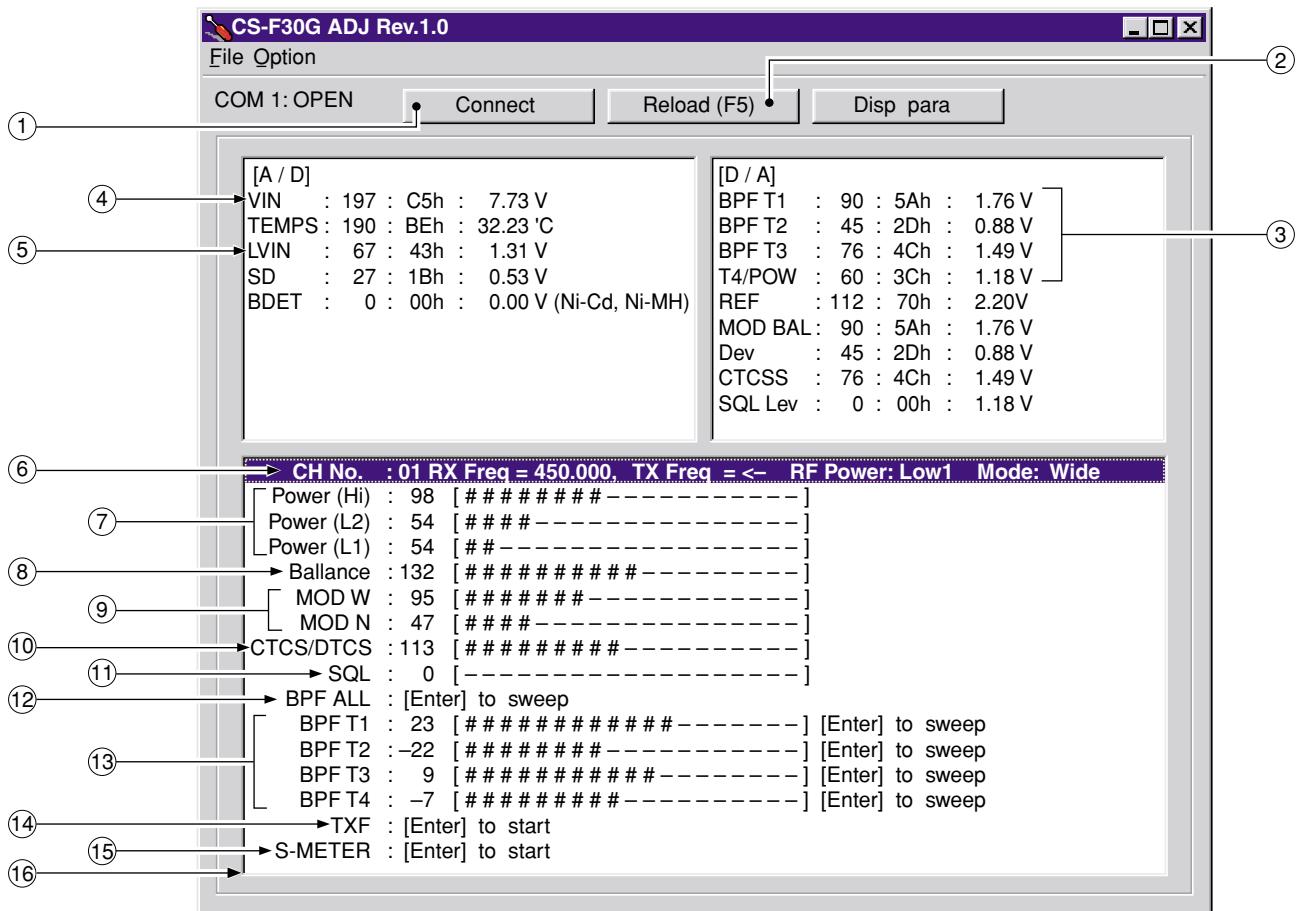
• Connection



• *OPC-966 (JIG CABLE)



• Screen display example



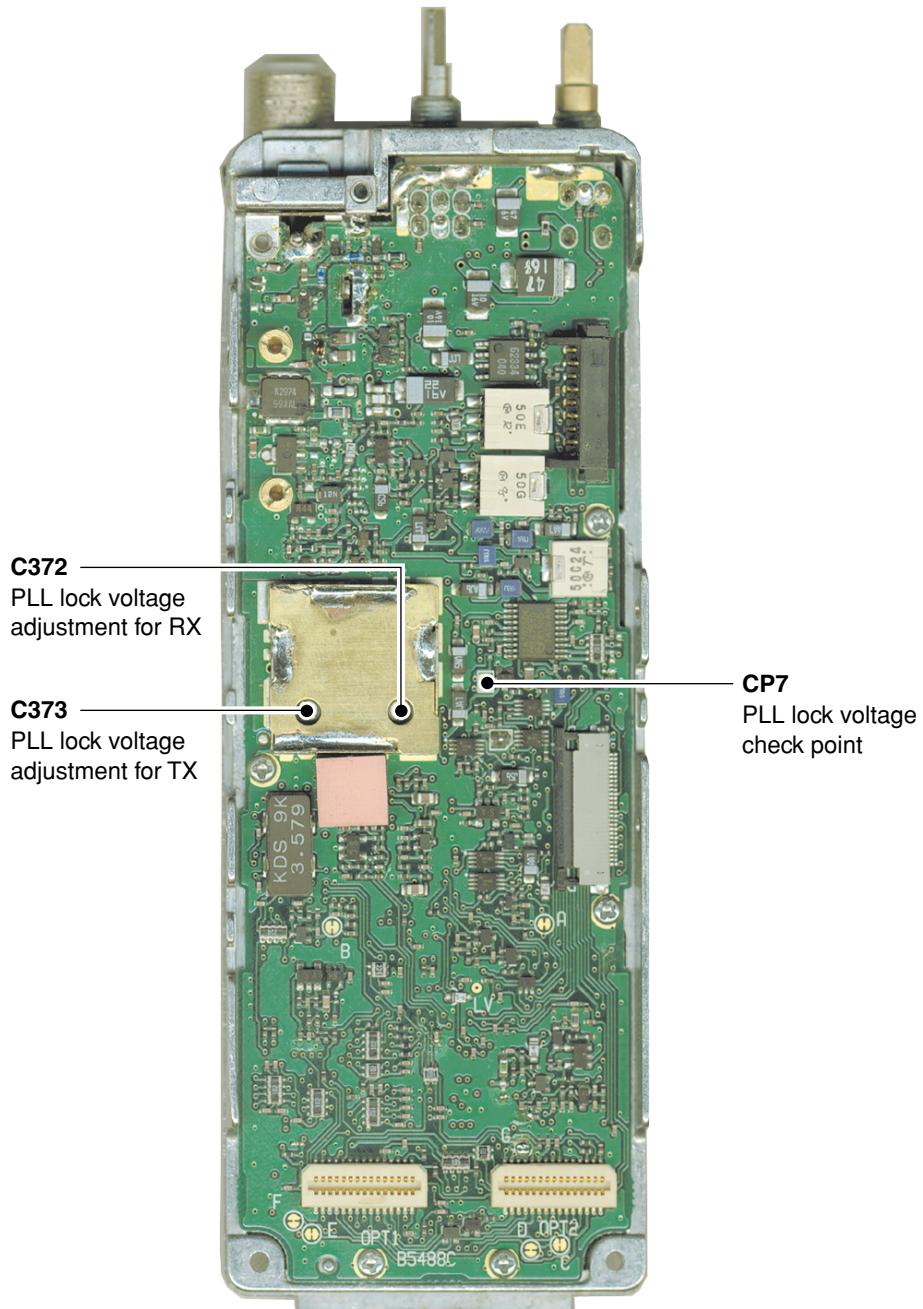
NOTE: The above values for settings are example only.
Each transceiver has its own specific values for each setting.

- | | |
|---------------------------------------|--|
| (1) : Transceiver's connection state | (9) : FM deviation |
| (2) : Reload adjustment data | (10) : CTCSS/DTCS deviation |
| (3) : Receive sensitivity measurement | (11) : Squelch level |
| (4) : Connected DC voltage | (12) : Receive sensitivity (automatically) |
| (5) : PLL lock voltage | (13) : Receive sensitivity (manually) |
| (6) : Operating channel select | (14) : Reference frequency |
| (7) : RF output power | (15) : S-meter |
| (8) : Modulation balance | (16) : Adjustment items |

5-2 PLL ADJUSTMENT

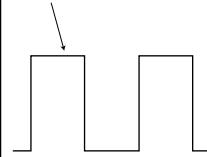
ADJUSTMENT		ADJUSTMENT CONDITIONS		MEASUREMENT		VALUE	ADJUSTMENT			
				UNIT	LOCATION		UNIT	ADJUST		
PLL LOCK VOLTAGE	1	<ul style="list-style-type: none"> • Operating freq. : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] • Receiving 		MAIN	Connect a digital multimeter or an oscilloscope to the check point, "CP7".	1.3 V	MAIN	C372		
	2	<ul style="list-style-type: none"> • Transmitting 				1.3 V		C373		
	3	<ul style="list-style-type: none"> • Operating freq. : 430.000 MHz [L] 480.000 MHz [ML] 490.000 MHz [MH] 520.000 MHz [H] • Receiving 				2.5–4.0 V [L] 3.0–4.5 V other		Verify		
	4	<ul style="list-style-type: none"> • Transmitting 				3.0–4.5 V				

- MAIN unit



5-3 SOFTWARE ADJUSTMENT

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	LOCATION	
REFERENCE FREQUENCY [TXF]	1	<ul style="list-style-type: none"> • Operating freq. : 430.000 MHz [L] 480.000 MHz [ML] 490.000 MHz [MH] 512.000 MHz [H]-USA 520.000 MHz [H]-other • Output power : Low1 • Connect the RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting 	Top panel	Loosely couple a frequency counter to the antenna connector.	430.0000 MHz [L] 480.0000 MHz [ML] 490.0000 MHz [MH] 512.0000 MHz [H]-USA 520.0000 MHz [H]-other
OUTPUT POWER [Power (Hi)]	1	<ul style="list-style-type: none"> • Operating freq. : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] • Output power : High • Transmitting 	Top panel	Connect an RF power meter to the antenna connector.	4.0 W
[Power (L2)]	2	<ul style="list-style-type: none"> • Output power : Low2 • Transmitting 			2.0 W
[Power (L1)]	3	<ul style="list-style-type: none"> • Output power : Low1 • Transmitting 			1.0 W
MODULATION BALANCE [Ballance]	1	<ul style="list-style-type: none"> • Operating freq. : 415.000 MHz [L] 460.000 MHz [ML] 470.000 MHz [MH] 496.000 MHz [H]-USA 500.000 MHz [H]-other • Output power : Low1 • Set the FM deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis: OFF Detector : (P-P)/2 • Push [P0] key while transmitting 	Top panel	Connect an FM deviation meter with an oscilloscope to the antenna connector through an attenuator.	Set to square wave form 
FM DEVIATION [MOD W]	1	<ul style="list-style-type: none"> • Operating freq. : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] • Output power : Low1 • IF bandwidth : Wide • Set the FM deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis: OFF Detector : (P-P)/2 • Connect the audio generator to the multi connector through the JIG cable (*OPC-966) and set as: 1.0 kHz/150 mVrms • Transmitting 	Top panel	Connect an FM deviation meter to the antenna connector through the attenuator.	±4.1 kHz
[MOD N]	2	<ul style="list-style-type: none"> • IF bandwidth : Narrow • Transmitting 			±2.1 kHz

SOFTWARE ADJUSTMENT – continued

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
CTCSS/DTCS DEVIATON [CTCS/DTCS]	<ul style="list-style-type: none"> • Operating freq. : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] • Output power : Low1 • IF bandwidth : Wide • CTCSS : 88.5 Hz • DTCS code : 007 • Set the FM deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis: OFF Detector : (P-P)/2 • No audio applied to the [MIC] input. • Transmitting 	Top panel	Connect an FM deviation meter to the antenna connector through the attenuator.	0.7 kHz
RX SENSITIVITY [BPF T1] – [BPF T4]	<ul style="list-style-type: none"> • Operating freq. : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] • IF bandwidth : Wide • Connect a standard signal generator to the antenna connector and set as: Frequency : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] Level : 10 µV* (-87 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving 	MAIN	Connect a SINAD meter with an 8 Ω load to the multi connector through the JIG cable (*OPC-966).	Minimum distortion level
	CONVENIENT: The BPF T1–BPF T4 can be adjusted automatically. ①-1: Set the cursor to “BPF ALL” on the adjustment program and then push [ENTER] key. ①-2: The connected PC tunes BPF T1–BPF T4 to peak levels. or ②-1: Set the cursor to one of BPF T1, T2, T3, or T4 as desired. ②-2: Push [ENTER] key to start tuning. ②-3: Repeat ②-1 and ②-2 to perform additional BPF tuning.			
S-METER [S-METER]	<ul style="list-style-type: none"> • Operating freq. : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] • IF bandwidth : Wide • Connect an SSG to the antenna connector and set as: Frequency : 400.000 MHz [L] 440.000 MHz [ML] 450.000 MHz [MH] 480.000 MHz [H] Level : 14 µV* (-84 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving 	MAIN		Push [ENTER] key on the connected computer keyboard to set “S3 level”.
	<ul style="list-style-type: none"> • Set an SSG as : Level : 0.45 µV* (-114 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving 			Push [ENTER] key on the connected computer keyboard to set “S1 level”.

*The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

SOFTWARE ADJUSTMENT – continued

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
SQUELCH LEVEL [SQL]	1 <ul style="list-style-type: none"> • Operating freq. : 415.000 MHz [L] 460.000 MHz [ML] 470.000 MHz [MH] 496.000 MHz [H]-USA 500.000 MHz [H]-other • IF bandwidth : Wide • Connect an SSG to the antenna connector and set as: <ul style="list-style-type: none"> Frequency : 415.000 MHz [L] 460.000 MHz [ML] 470.000 MHz [MH] 496.000 MHz [H]-USA 500.000 MHz [H]-other Level : 0.2 µV* (-121 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving 	Front panel	Internal speaker	<p>Set “SQL level” to close squelch.</p> <p>Then set “SQL level” at the point where the audio signals just appears.</p>

*The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

SECTION 6 PARTS LIST

[FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	
IC1	1130009860	S.IC	TC74VHC373FT (EL)
Q1	1530002850	S.TRANSISTOR	2SC4116-BL (TE85R)
Q2	1530002850	S.TRANSISTOR	2SC4116-BL (TE85R)
Q3	1590002150	S.TRANSISTOR	DTC144TE TL
Q4	1590002150	S.TRANSISTOR	DTC144TE TL
Q5	1590002150	S.TRANSISTOR	DTC144TE TL
Q6	1560001130	S.FET	CPH3403-TL
Q7	1560001130	S.FET	CPH3403-TL
Q8	1530002060	S.TRANSISTOR	2SC4081 T107 R
Q9	1590000430	S.TRANSISTOR	DTC144EUA T106
D1	1790001280	S.DIODE	MA111 (TX)
D2	1790001280	S.DIODE	MA111 (TX)
D3	1790001200	S.DIODE	MA6S121 (TX)
D4	1790001280	S.DIODE	MA111 (TX)
R1	7030007300	S.RESISTOR	ERJ2GEJ 332 X (3.3 kΩ)
R2	7030005030	S.RESISTOR	ERJ2GEJ 152 X (1.5 kΩ)
R3	7030007250	S.RESISTOR	ERJ2GEJ 220 X (22 Ω)
R4	7030009150	S.RESISTOR	ERJ2GEJ 824 X (820 kΩ)
R5	7030009150	S.RESISTOR	ERJ2GEJ 824 X (820 kΩ)
R6	7030006610	S.RESISTOR	ERJ2GEJ 394 X (390 kΩ)
R7	7030008310	S.RESISTOR	ERJ2GEJ 564 X (560 kΩ)
R8	7030008370	S.RESISTOR	ERJ2GEJ 561 X (560 Ω)
R9	7030004990	S.RESISTOR	ERJ2GEJ 221 X (220 Ω)
R10	7030005030	S.RESISTOR	ERJ2GEJ 152 X (1.5 kΩ)
R11	7030007300	S.RESISTOR	ERJ2GEJ 332 X (3.3 kΩ)
R12	7030005060	S.RESISTOR	ERJ2GEJ 333 X (33 kΩ)
R13	7030007280	S.RESISTOR	ERJ2GEJ 331 X (330 Ω)
R14	7030005090	S.RESISTOR	ERJ2GEJ 104 X (100 kΩ)
R17	7030005090	S.RESISTOR	ERJ2GEJ 104 X (100 kΩ)
R18	7410000750	S.ARRAY	EXB-V4V 104JV (100 kΩ)
R19	7030005050	S.RESISTOR	ERJ2GEJ 103 X (10 kΩ)
R20	7030005170	S.RESISTOR	ERJ2GEJ 474 X (470 kΩ)
R21	7030005090	S.RESISTOR	ERJ2GEJ 104 X (100 kΩ)
R22	7030005170	S.RESISTOR	ERJ2GEJ 474 X (470 kΩ)
C1	4030016930	S.CERAMIC	ECJ0EB1A104K
C2	4030016930	S.CERAMIC	ECJ0EB1A104K
C3	4030016930	S.CERAMIC	ECJ0EB1A104K
C4	4550006150	S.TANTALUM	ECST1CY105R
C6	4550006150	S.TANTALUM	ECST1CY105R
C7	4550006150	S.TANTALUM	ECST1CY105R
C8	4550006150	S.TANTALUM	ECST1CY105R
C9	4550006150	S.TANTALUM	ECST1CY105R
C10	4550006150	S.TANTALUM	ECST1CY105R
C11	4550006150	S.TANTALUM	ECST1CY105R
C12	4030014180	S.CERAMIC	ECUE1H470JCQ
C13	4030014180	S.CERAMIC	ECUE1H470JCQ
C14	4030014180	S.CERAMIC	ECUE1H470JCQ
C15	4030014180	S.CERAMIC	ECUE1H470JCQ
C16	4030013850	S.CERAMIC	ECUE1E102KBQ
C17	4030014180	S.CERAMIC	ECUE1H470JCQ
C18	4030014180	S.CERAMIC	ECUE1H470JCQ
C19	4030016930	S.CERAMIC	ECJ0EB1A104K
C20	4030014180	S.CERAMIC	ECUE1H470JCQ
C21	4550006150	S.TANTALUM	ECST1CY105R
C22	4030016930	S.CERAMIC	ECJ0EB1A104K
C23	4550006150	S.TANTALUM	ECST1CY105R
C24	4030014430	S.CERAMIC	C1005 JB 1C 153K-T-A
C25	4030014180	S.CERAMIC	ECUE1H470JCQ
C26	4030016930	S.CERAMIC	ECJ0EB1A104K
J1	6510022360	S.CONNECTOR	26FLZ-SM1-TB
J2	6510022200	S.CONNECTOR	40FLZ-SM1-R-TB
DS1	5010000160	S.LED	LNJ310M6URA
DS2	5010000160	S.LED	LNJ310M6URA
DS3	5010000160	S.LED	LNJ310M6URA

[FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	
DS4	5010000160	S.LED	LNJ310M6URA
DS5	5040002170	S.LED	LNJ210C6ARA
DS6	5010000120	S.LED	LN1371G-(TR) [GT] only
DS7	5010000120	S.LED	LN1371G-(TR) [GT] only
DS8	5010000120	S.LED	LN1371G-(TR) [GT] only
DS9	5010000120	S.LED	LN1371G-(TR) [GT] only
DS10	5030001870	LCD	EDMMUD1FA0
DS11	5010000120	S.LED	LN1371G-(TR) [GT] only
DS12	5010000120	S.LED	LN1371G-(TR) [GT] only
DS13	5010000160	S.LED	LNJ310M6URA
DS14	5010000120	S.LED	LN1371G-(TR) [GS] only
DS15	5010000120	S.LED	LN1371G-(TR) [GS] only
MC1	7700002310	MICROPHONE	EM-140
S1	2230001060	S.SWITCH	EVQ-PUL 02K
S2	2230001060	S.SWITCH	EVQ-PUL 02K
S3	2230001060	S.SWITCH	EVQ-PUL 02K
S4	2230001060	S.SWITCH	EVQ-PUL 02K
S5	2230001060	S.SWITCH	EVQ-PUL 02K
SP1	2510001060	SPEAKER	K036NA500-47
W1	7120000470	JUMPER	ERDS2T0
EP1	0910052494	PCB	B 5489D [F40G]
	0910053635	PCB	B 5489E [F41G]

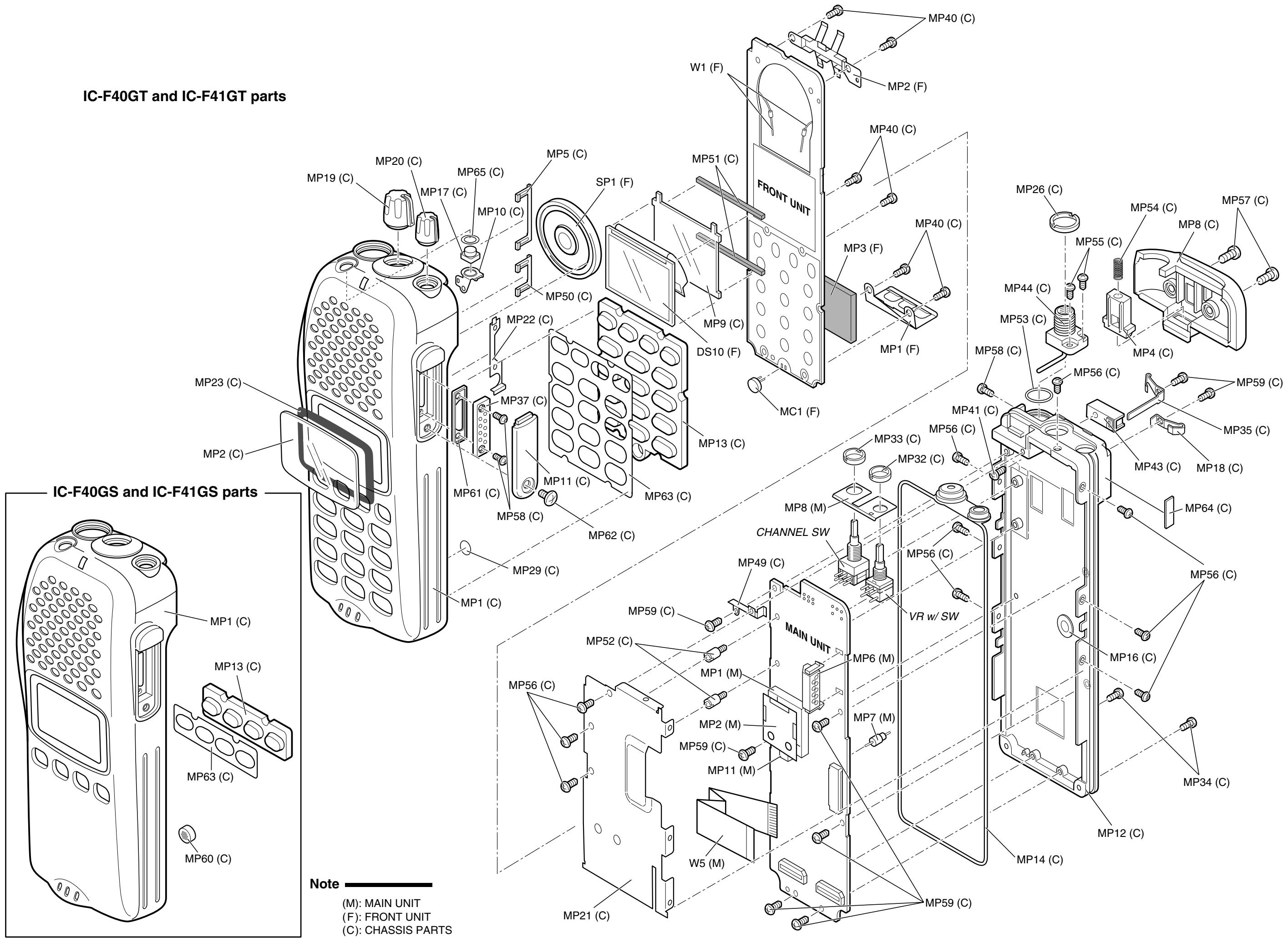
S.=Surface mount

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION		
C442	4030004820	S.CERAMIC	C2012 CH 1H 050C-T-A	[H]
	4030014030	S.CERAMIC	ECUE1H2R5BCQ	[L]
	4030014420	S.CERAMIC	ECUE1H0R5BCQ	[ML], [MH]
C443	4030013850	S.CERAMIC	ECUE1E102KBQ	
C444	4030014490	S.CERAMIC	ECUE1H331KBQ	
C445	4030013940	S.CERAMIC	C1005 JB 1C 223K-T-N	
C446	4030017250	S.CERAMIC	ECUE1E821KBQ	
C447	4030017250	S.CERAMIC	ECUE1E821KBQ	
C448	4030013850	S.CERAMIC	ECUE1E102KBQ	
C449	4030016930	S.CERAMIC	ECJ0EB1A104K	
C450	4030016930	S.CERAMIC	ECJ0EB1A104K	
C451	4030016930	S.CERAMIC	ECJ0EB1A104K	
C452	4030016930	S.CERAMIC	ECJ0EB1A104K	
C453	4030014140	S.CERAMIC	ECUE1H150JCQ	
C454	4030014240	S.CERAMIC	ECUE1H180JCQ	
C455	4030016930	S.CERAMIC	ECJ0EB1A104K	
C456	4030016930	S.CERAMIC	ECJ0EB1A104K	
C457	4030014070	S.CERAMIC	ECUE1H040BCQ	
C458	4030014200	S.CERAMIC	ECUE1H101JCQ	
C459	4030014180	S.CERAMIC	ECUE1H470JCQ	[F41G] only
C460	4030014130	S.CERAMIC	ECUE1H120JCQ	[F41G] only
C461	4030014080	S.CERAMIC	ECUE1H050BCQ	[F41G] only
C462	4030014080	S.CERAMIC	ECUE1H050BCQ	[F41G] only
C463	4030014180	S.CERAMIC	ECUE1H470JCQ	[F41G] only
C464	4030014180	S.CERAMIC	ECUE1H470JCQ	[F41G] only
C465	4030014180	S.CERAMIC	ECUE1H470JCQ	[F41G] only
C466	4030014180	S.CERAMIC	ECUE1H470JCQ	[F41G] only
C467	4030014080	S.CERAMIC	ECUE1H050BCQ	[F41G] only
C468	4030014080	S.CERAMIC	ECUE1H050BCQ	[F41G] only
C469	4030014080	S.CERAMIC	ECUE1H050BCQ	[F41G] only
C470	4030014080	S.CERAMIC	ECUE1H050BCQ	[F41G] only
C471	4030014180	S.CERAMIC	ECUE1H470JCQ	[F41G] only
C472	4030014180	S.CERAMIC	ECUE1H470JCQ	[F41G] only
C473	4550006700	S.TANTALUM	ECST1AY106R	[F41G] only
C474	4030009520	S.CERAMIC	C1608 CH 1H 020B-T-A	[H] only
J1	6510018430	S.CONNECTOR	AXN330C038P	
J2	6510018430	S.CONNECTOR	AXN330C038P	
J3	6510022360	S.CONNECTOR	26FLZ-SM1-TB	
F1	5210000710	S.FUSE	KAB 2402 322 NA29	
S1	2250000180	ENCODER	EC10SP16-47	
W2	7030003860	S.JUMPER	ERJ3GE JPW V	
W3	7030003860	S.JUMPER	ERJ3GE JPW V	
W5	8900009790	CABLE	OPC-972	
W7	7030003860	S.JUMPER	ERJ3GE JPW V	
W8	7030009970	S.JUMPER	MJ-0.1	
W9	7030003860	S.JUMPER	ERJ3GE JPW V	
W10	7030000010	S.JUMPER	MCR10EZHZ JPW (000)	
W11	7030010040	S.JUMPER	ERJ2GE-JPW	
W12	7030010040	S.JUMPER	ERJ2GE-JPW	[F40G] only
W13	7030003860	S.JUMPER	ERJ3GE JPW V	[H] only
EP1	0910052503	PCB	B 5488C	[F40G]
EP2	0910053620	PCB	B 5619	[F41G]
	6910013350	S.BEAD	BLM10A121S	[F41G] only

S.=Surface mount

IC-F40GT and IC-F41GT parts



SECTION 8 SEMI-CONDUCTOR INFORMATION

8 - 1 TRANSISTORS AND FETS

NAME	SYMBOL	INSIDE VIEW
2SA1362 GR	AEG	
2SB1132 R	BARB	
2SC3585 R44 2SC4081 R 2SC4116 BL 2SC4213 B 2SC4215 O 2SC4226 R25 2SC5107 O	R44 BR LL AB QO R25 MFO	
2SK880-Y	XY	
2SK1829	K1	
2SK2973	K1	
2SK2974	K2974	(TOP VIEW)

NAME	SYMBOL	INSIDE VIEW
3SK166A-2 3SK293	K UF	
CPH3403-TL	KD	
DTA144EUA	16	
DTC144EUA	26	
DTC144TE TL	06	
UN911H	6P	
XP6501 AB	5N	
XP1214	9H	

8 - 2 DIODES

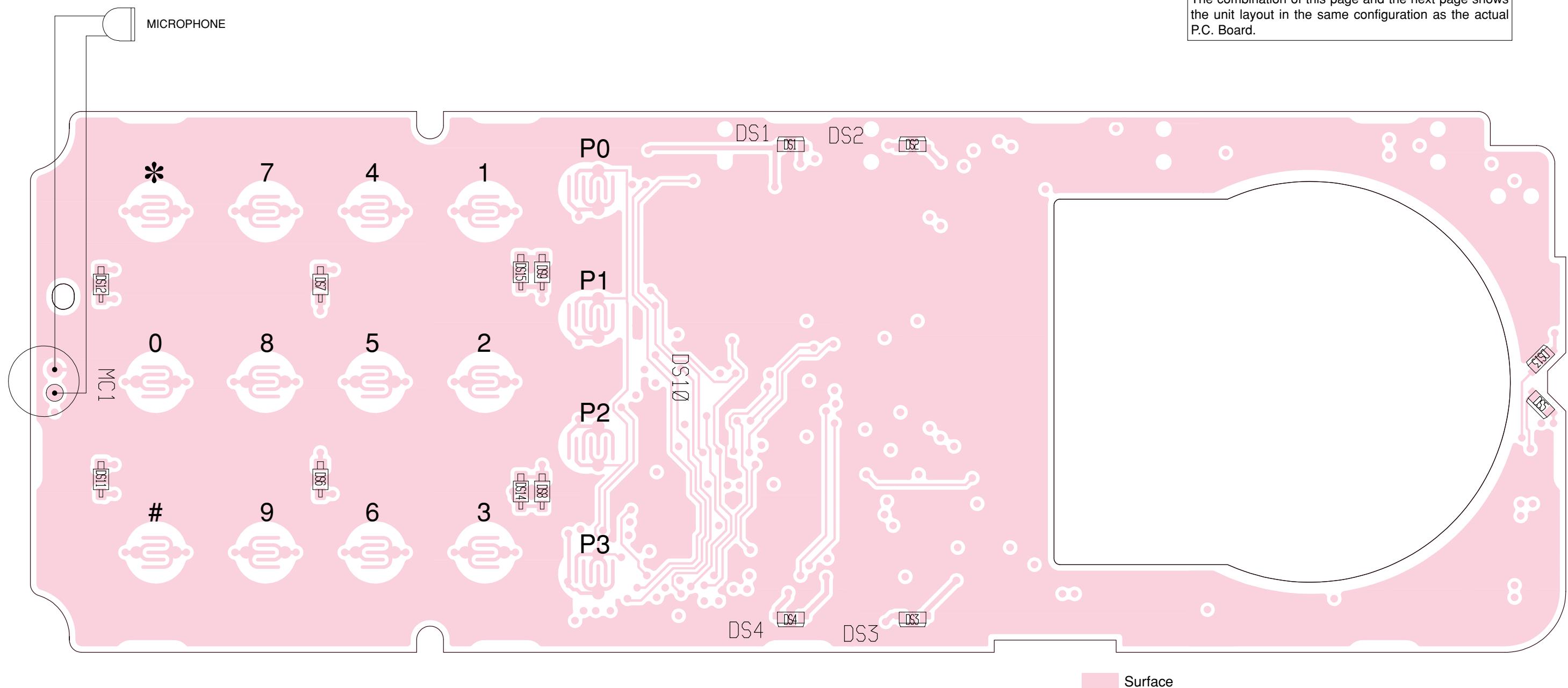
NAME	SYMBOL	INSIDE VIEW
1SS355 1SV307	A TX	
1SS375 MA742 RB706F-40	FH M1U 3J	
1T365-01	PINK LINE	
DAN202U	N	
DAP202U	P	
HSU88TRF MA111 MA2S111 MA8030-H MA8033-H MA8062-M	9 1B A 3^0 3^3 6-2	
HVC375BTRF HVU350TRF	6B 4	

NAME	SYMBOL	INSIDE VIEW
MA6S121	M2D	
MA77	4B	

SECTION 9 BOARD LAYOUTS

9 - 1 F40G FRONT UNIT

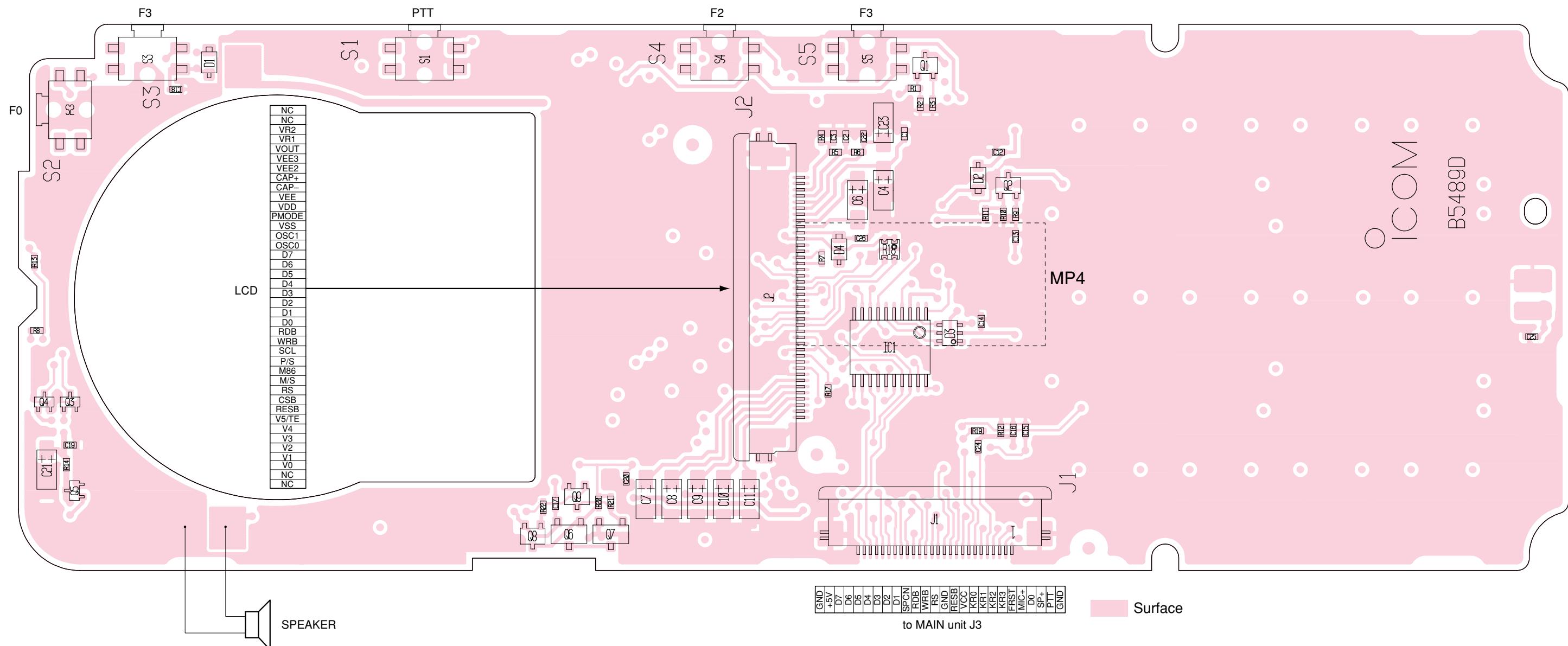
• TOP VIEW



F40G (FRONT unit)

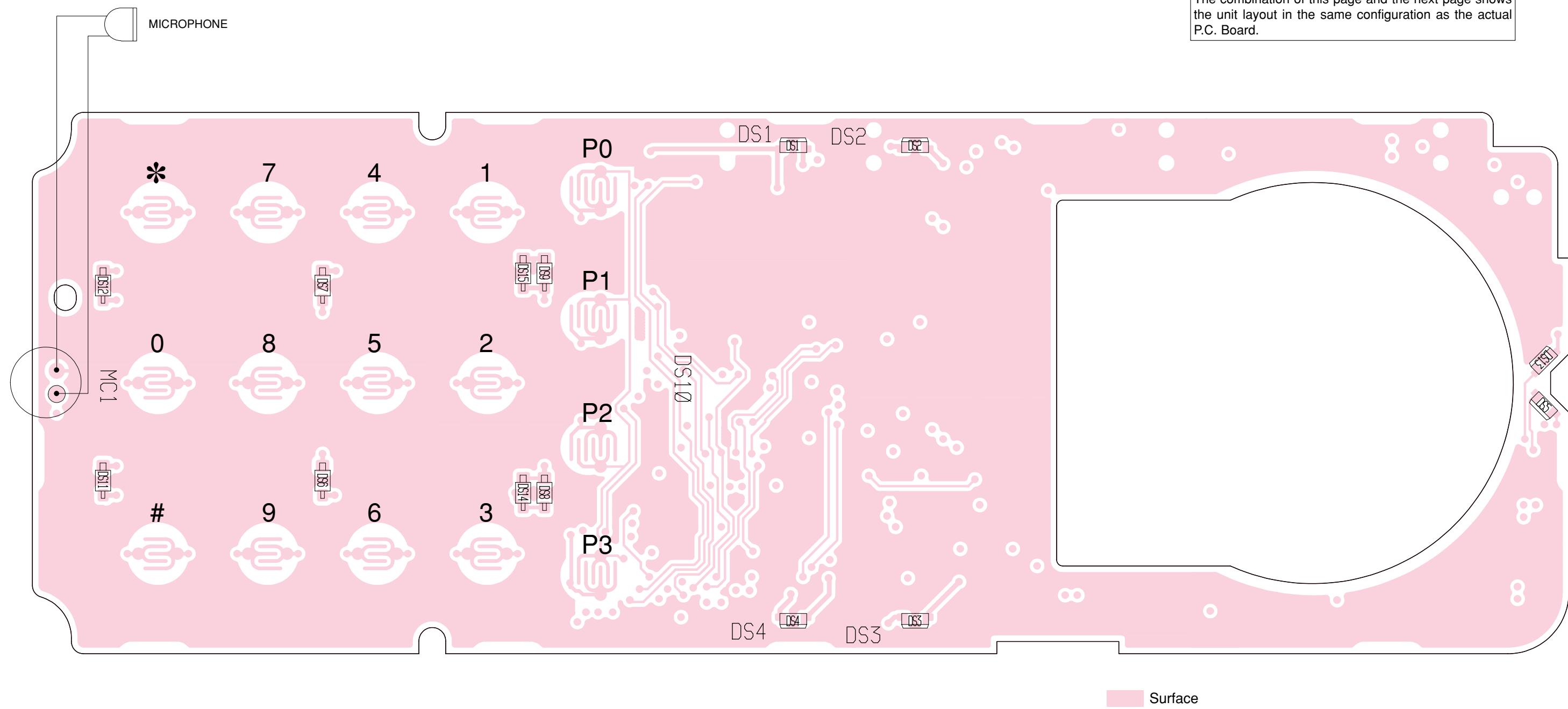
• BOTTOM VIEW

The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.



9 - 2 F41G FRONT UNIT

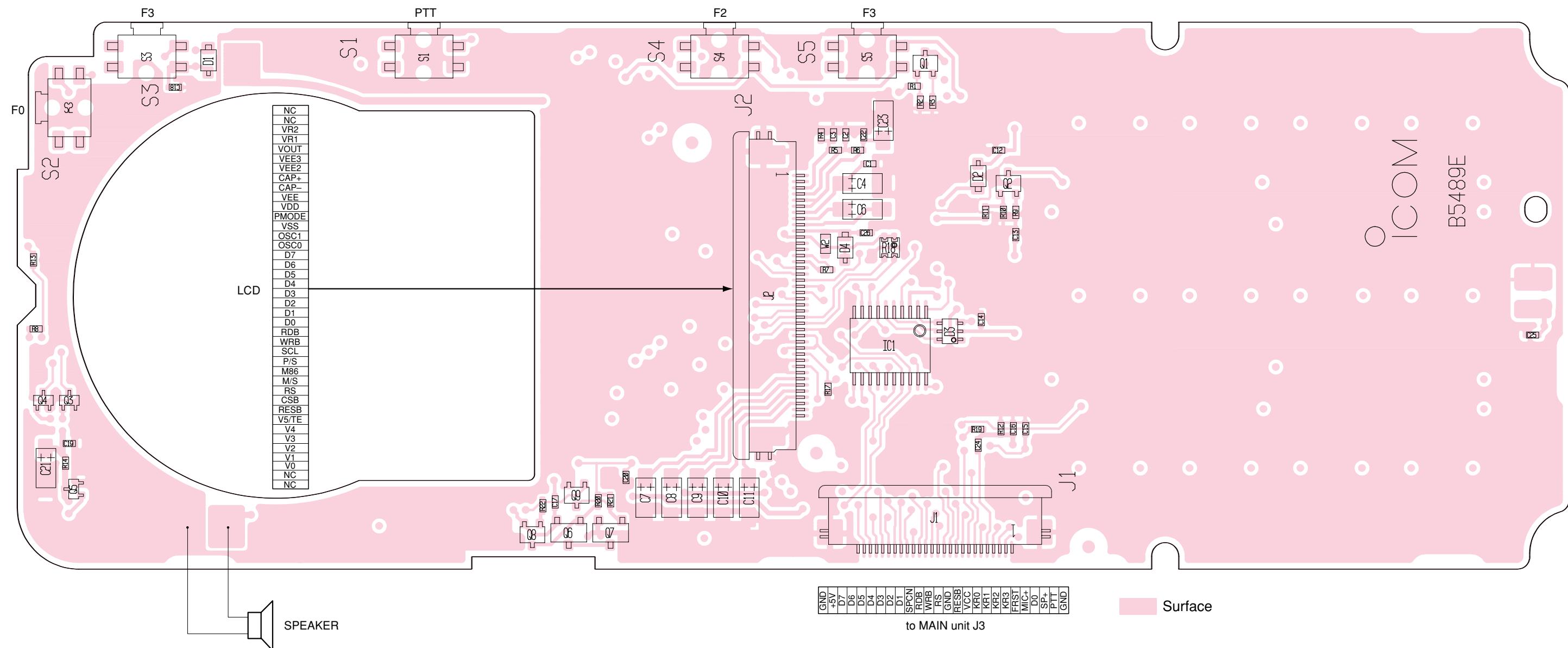
• TOP VIEW



F41G (FRONT unit)

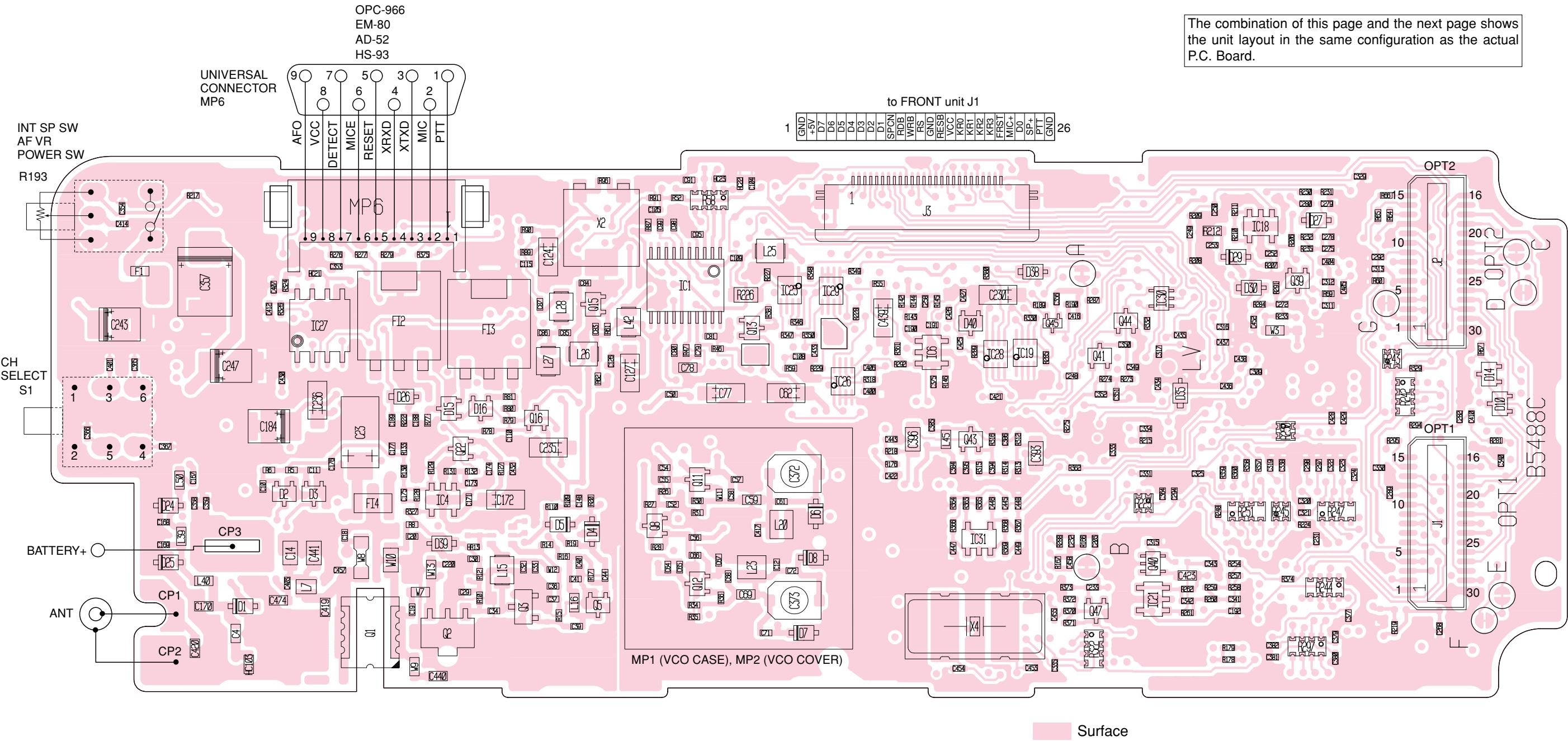
• BOTTOM VIEW

The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.



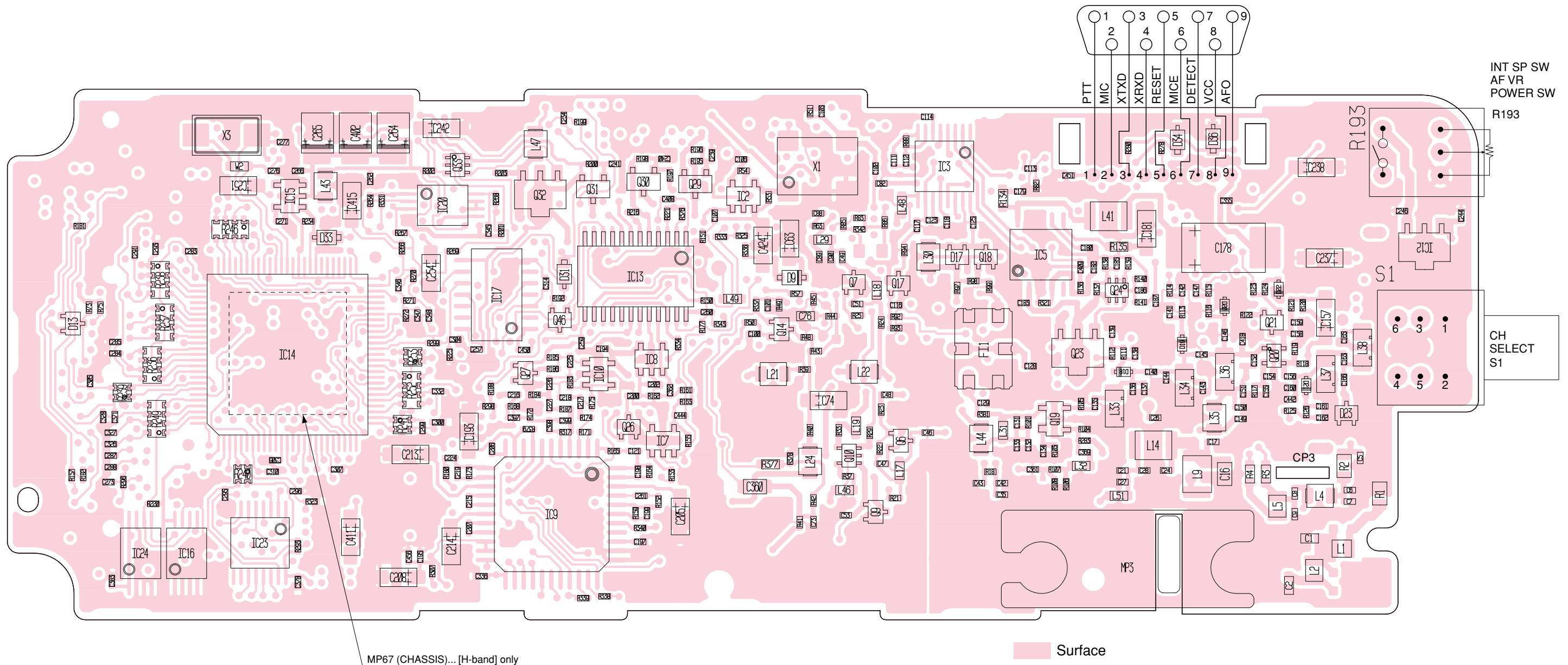
9 - 3 F40G MAIN UNIT

• TOP VIEW



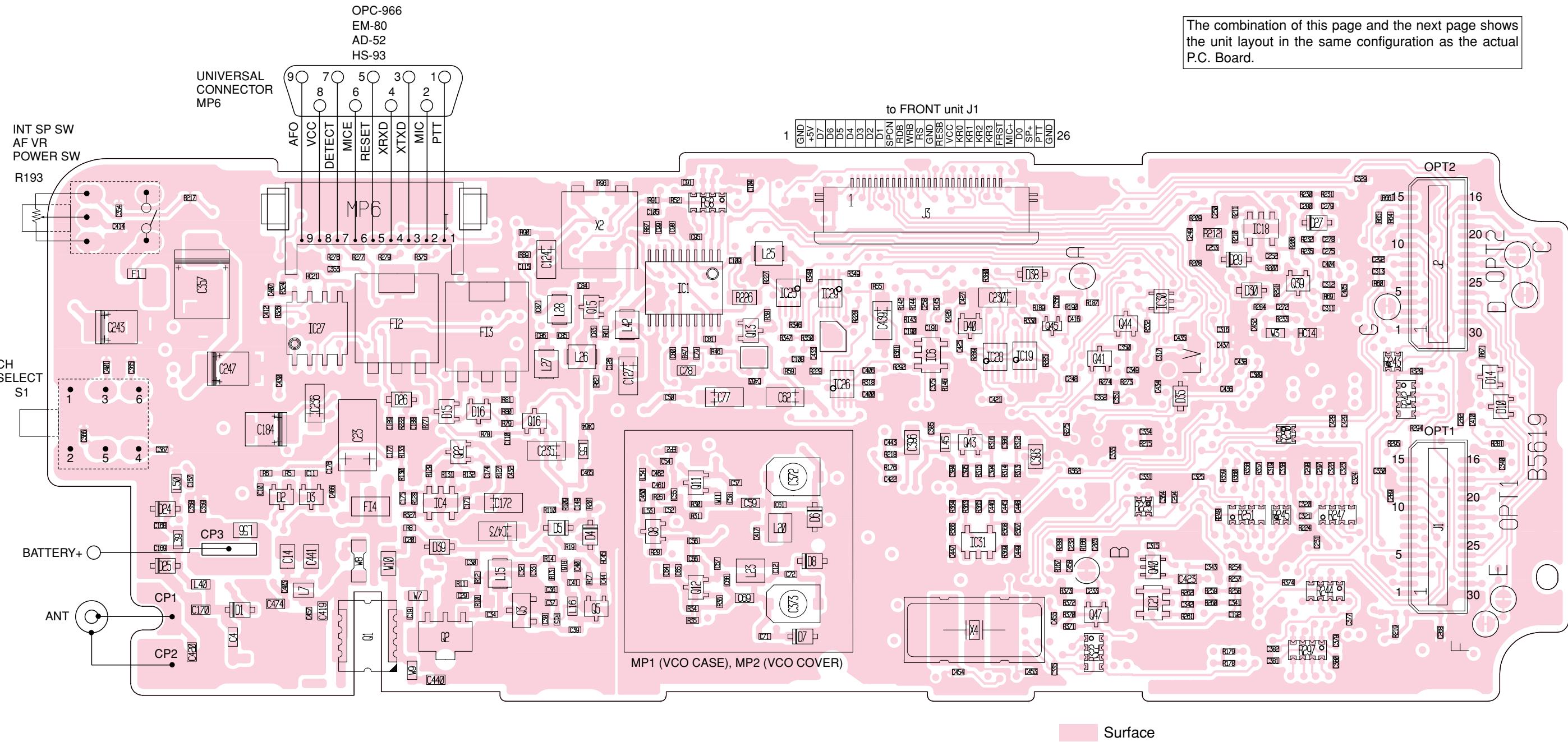
F40G (MAIN unit)
• BOTTOM VIEW

The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.



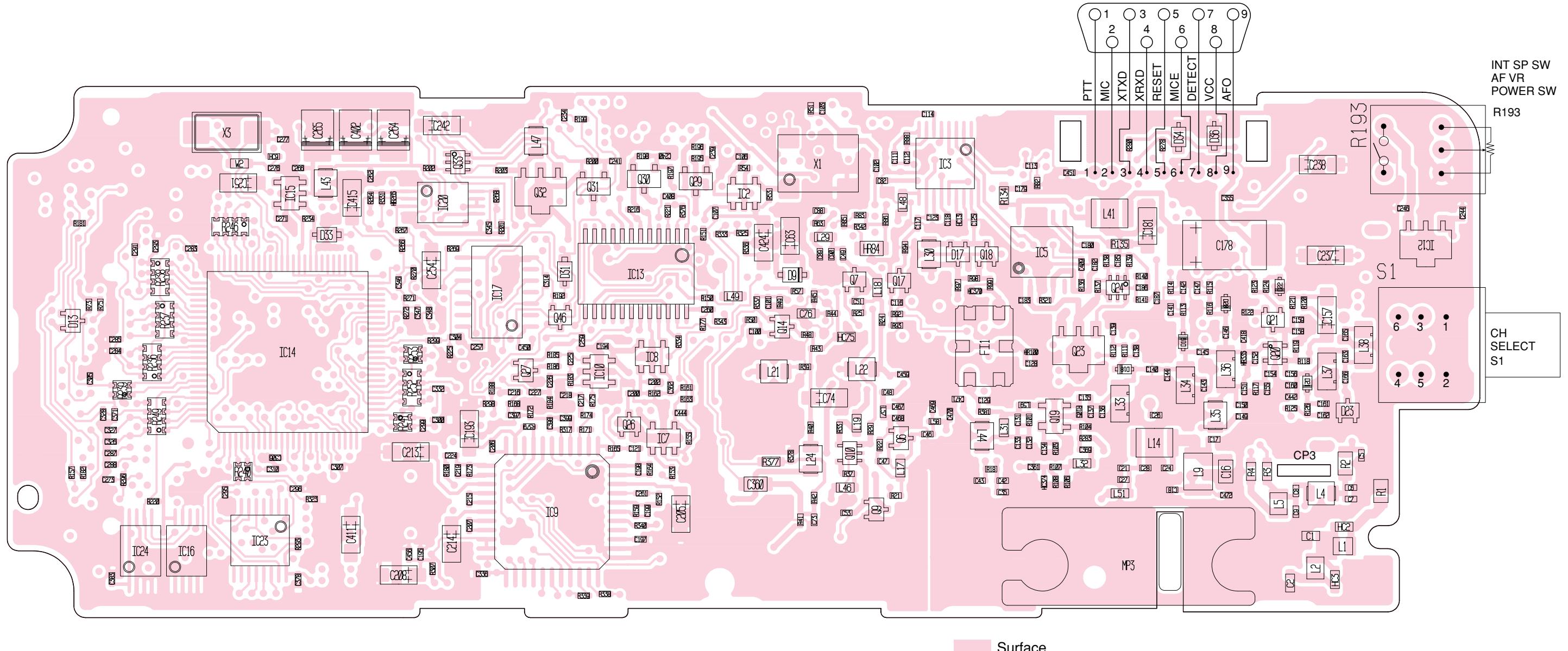
9 - 4 F41G MAIN UNIT

• TOP VIEW

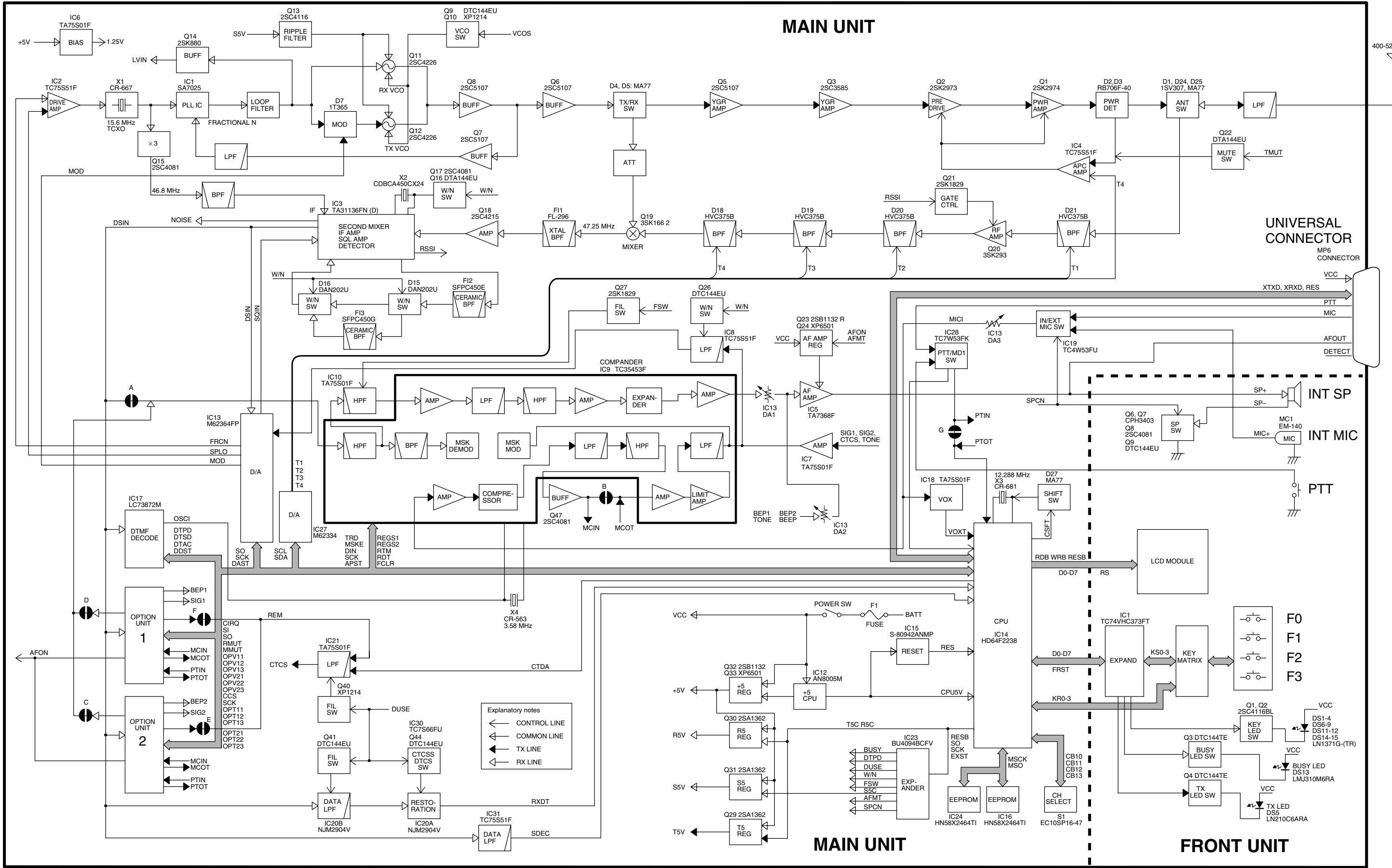


F41G (MAIN unit)
• BOTTOM VIEW

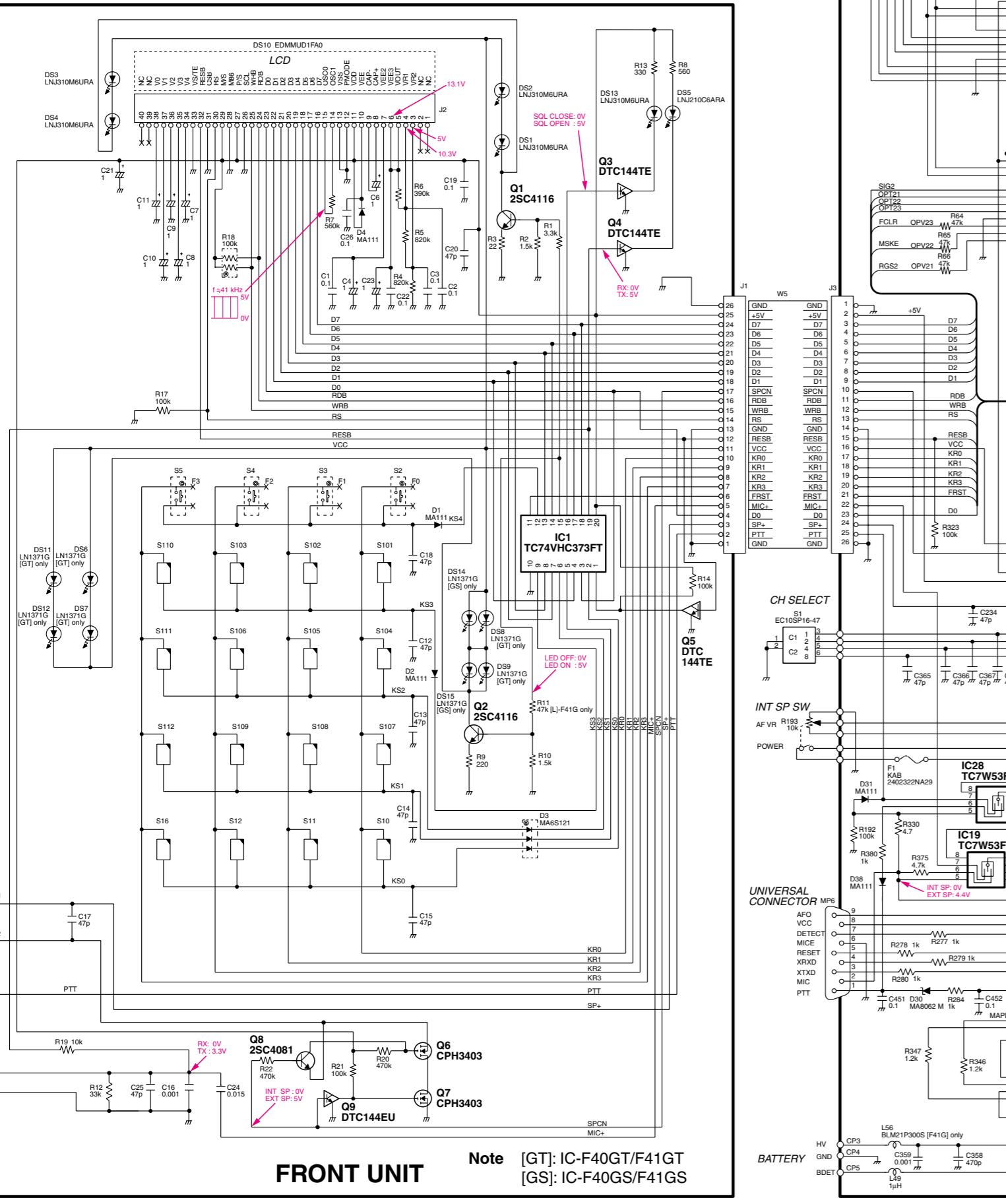
The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.



SECTION 10 BLOCK DIAGRAM

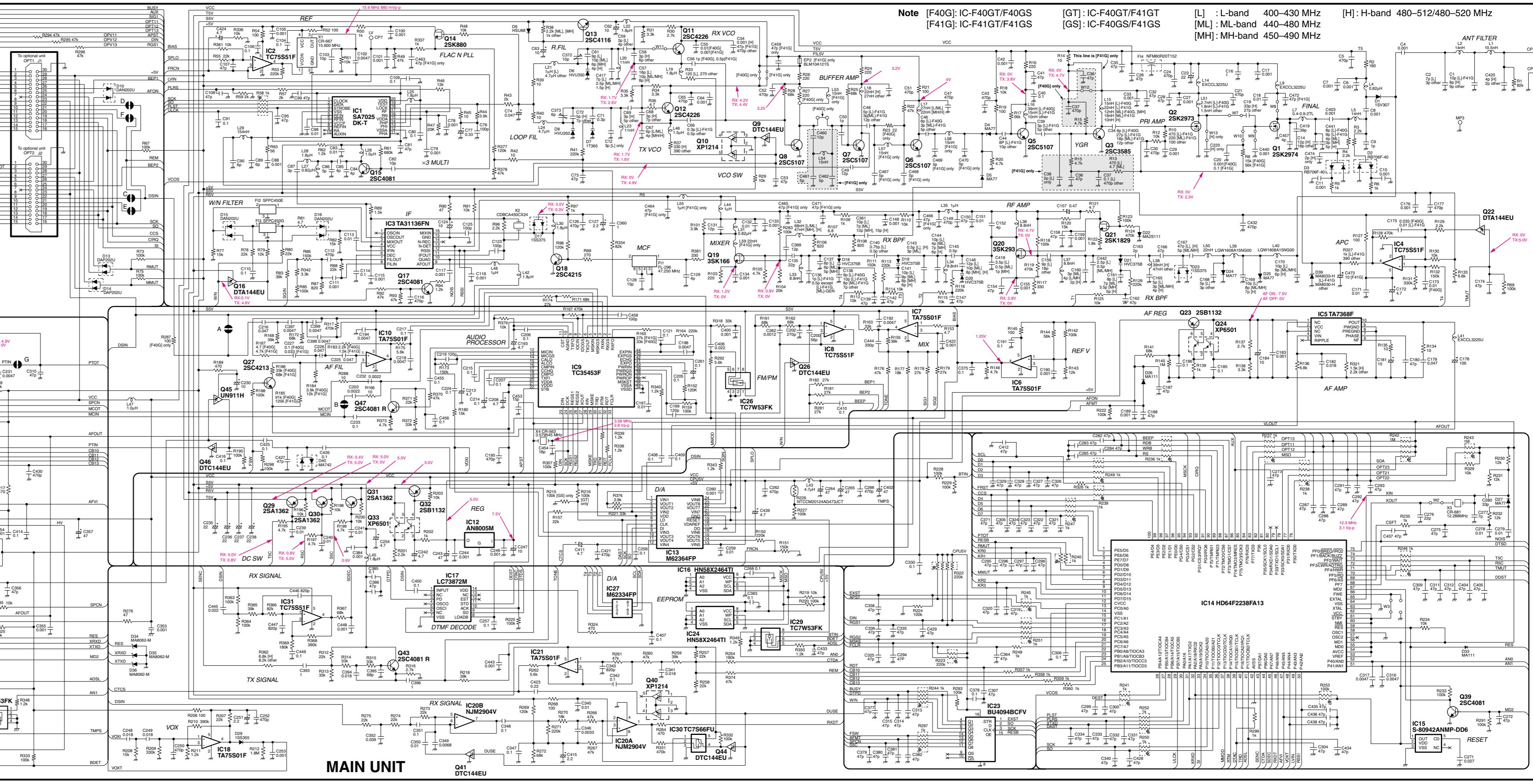


SECTION 11 VOLTAGE DIAGRAM



FRONT UNIT

Note [GT]: IC-F40GT/F41GT
[GS]: IC-F40GS/F41GS



MAIN UNIT

Note [F40G]: IC-F40GT/F40GS
[F41G]: IC-F41GT/F41GS
[GT]: IC-F40GT/F41GT
[GS]: IC-F40GS/F41GS

[L] : L-band 400~430 MHz
[ML] : ML-band 440~480 MHz
[MH] : MH-band 450~490 MHz

[H] : H-band 480~512/480~520 MHz

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Count on us!